

FINAL ENGINEERING REPORT  
FOR THE  
MEDIUM RESOLUTION INFRA-RED (MRIR) EXPERIMENT  
ENGINEERING MODEL DIGITAL ELECTRONICS TELEMETRY UNIT  
FOR  
NIMBUS "B"

1 November 1965 - 1 April 1966

CONTRACT NO. NAS5-9699

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## SUMMARY

The object of this report is to describe in detail the overall design aspects of the Engineering Model MRIR Telemetry Unit, and to present design information on the Bench Test Equipment which was modified for the MRIR Telemetry Unit. The Bench Test Equipment was originally designed and fabricated for the MRIR Telemetry Unit contained in the NIMBUS "C" Spacecraft.

The final engineering design report is intended to establish information on the telemetry unit operation, to define engineering problems uncovered during functional testing, and to recommend improvements to be incorporated into succeeding units. Data pertinent to maintaining the MRIR Telemetry Unit is also presented within this report.

The finished Engineering Model MRIR Telemetry Unit had slight deviations from the information presented in the Design Study Report, CalComp Document D0301-013, dated 31 December 1965. The deviations, electrical in nature, were brought about because of problems uncovered during functional test. These problems involved circuit changes or logic changes. These were as follows:

- a. Noise pulses on the second stage flip-flop input of the commutation ring counter.

- b. 200-kc input filter network.
- c. A/D Converter comparator amplifier compensation.
- d. A/D Converter precision operational amplifier compensation.
- e. MOS-FET device failures during functional test.

Solutions and recommendations pertaining to these problems are explained in the main test of this report.

The initial engineering model design approach was straightforward and relatively complete. Except for necessary changes to ensure reliable operation, only two recommendations are made as improvements. One improvement recommendation is the availability of two MOS-FET devices per analog input channel (requires two additional TO-5 packages), and the other improvement is to provide better noise isolation on the second stage commutation ring counter.

The functional test of the Engineering Model MRIR Telemetry Unit was performed with the aid of the modified NIMBUS "C" Bench Test Equipment. The BTE provided the input signals and captured the responses which were processed to provide visual inspection capability for determining the operation of the telemetry unit. Inasmuch as the BTE was used to test the telemetry unit, the very act of its testing capability provided data which indicated that the BTE was performing in a manner which constituted acceptance of its own operability. Therefore, the modification to the BTE has been tested through actual use of the equipment.

In concluding this summary, it is felt that the Engineering Model MRIR Telemetry Unit and the Bench Test Equipment meet the requirements of the GSFC-NASA specification for the Medium Resolution IR (MRIR) Experiment Engineering Model for the NIMBUS "B" Spacecraft. The design, fabrication, assembly, and testing of the telemetry unit did not present any major problems that could not be simply and easily rectified. The mechanical design is complete and all parts were assembled without any modifications being required. With the inclusion of the suggested recommendations, prototype and flight model telemetry units may be constructed and tested in the same manner as the Engineering Model MRIR Telemetry Unit. The BTE and its new modifications have been checked out and found to be sufficient for testing the telemetry unit. No further additions or modifications are to be incorporated into the BTE.

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## SECTION 1

### INTRODUCTION

The Engineering Model MRIR Telemetry Unit has been designed, fabricated, functionally tested, and delivered. A final engineering report covering the history, fabrication, and testing of the completed subsystem is presented herein. In addition, this report shall cover the Bench Test Equipment which was modified for the NIMBUS "B" telemetry unit.

#### 1.1 SCOPE

This final report contains the data which is pertinent to the completed Engineering Model MRIR Telemetry Unit. The report is intended to cover the electrical, mechanical, and functional testing aspects of the completed subsystem, provide recommendations for improvement on following units, and to provide sufficient data for maintenance purposes. Also, a functional and physical description of the modified Bench Test Equipment shall be included in this report.

#### 1.2 HISTORY OF CONTRACT NAS5-9699

A CPIF contract with an incentive clause for cost and delivery was awarded to California Computer Products, Inc.,

(CalComp) on 1 November 1965. The overall object of the contract was to perform a design study on a Medium Resolution Infra-red (MRIR) Telemetry Unit which had been designed by NASA for the NIMBUS "B" Spacecraft, to review and recommend improvements in the design, and to generate a pre-prototype engineering model based on the results presented and agreed to in the design study review. In addition to the telemetry unit, the contract required that one set of NIMBUS "C" MRIR-PCM Bench Test Equipment (BTE) be modified for use with the NIMBUS "B" Telemetry Unit. Manuals to support the BTE for both operation and maintenance purposes were also required as part of this contract. The contract called for completion of the hardware fabrication and final delivery on or before 31 March 1966.

The delivery of the Engineering Model MRIR Telemetry Unit was fulfilled with a final sell-off demonstration test to an authorized representative of the Government as appointed by NASA on 1 April 1966.

To aid in the design study of the MRIR Telemetry Unit, NASA shipped to California Computer Products, a breadboard version of the design on 9 November 1965. The breadboard consisted of two major parts, the power supply and the telemetry unit logic section with associated drawings and test aids. With the aid of the breadboard, careful analysis and relying on the past experience of the NIMBUS "C" MRIR Telemetry Unit, CalComp generated a design study report which assessed the submitted design for the proposed

telemetry unit. The design study report pointed out potential trouble areas, recommended improvements, and presented a hardware packaging concept with thermal and mechanical analytical data.

The preliminary design study report was submitted to NASA on 31 December 1965 for their review. On 6 January 1966, three representatives from NASA consisting of the contracting officer, the technical officer, and the telemetry unit designer met with CalComp representatives at CalComp to discuss the recommendations set forth in the design study report. At this meeting, it was determined what recommendations would be adopted. It was also decided that all suggested improvements which were adopted were within the scope of the original contract; therefore, no negotiations were required to receive additional funding for work considered to be beyond the intent of the original contract. With the formal approval of NASA on 25 February 1966, CalComp initiated the orders to produce an engineering model of the MRIR Telemetry Unit. Parts were ordered, artwork for the printed circuit modules was completed, functional test specifications were written, and supporting test equipment was developed and fabricated. The BTE design was firmed up as a result of the agreement reached on the MRIR design recommendations.

All parts contained within the Engineering Model MRIR Telemetry Unit were ordered from vendors with the exception of the flat pack integrated circuits which were Government-

furnished. The GFE IC's were functionally tested at CalComp prior to being soldered to the printed circuit boards.

On 2 March 1966, an interface agreement meeting conducted by General Electric was held at Goddard Space Flight Center in Greenbelt, Maryland. In attendance were representatives from General Electric, Santa Barbara Research, California Computer Products, Inc., and NASA. The purpose of the meeting was to establish interface requirements among the equipment suppliers. Since General Electric has the responsibility for system integration, General Electric conducted the meeting. The final results of the meeting were to be compiled into separate documents specifically directed to the participating equipment manufacturers.

After the establishment of interface requirements, the task at hand was to fabricate, assemble, and test the Engineering Model MRIR Telemetry Unit. The telemetry unit consists of a magnesium chassis and seven printed circuit cards. The procurement of parts for the assembly did not present delivery problems. The IC's were hand soldered to the printed circuit boards even though a resistive soldering machine was slated to be used for this job. Using the soldering machine, a sample IC board was prepared with dummy IC's which were attached to the printed circuit board. The sample was submitted to NASA for review and tests. NASA tests showed that the soldering was unsuitable at this time; however, NASA recommended several improvements in

using the soldering machine. The NASA laboratory report indicated that once the right combination of heat, solder content, solder deposition, and bonding pad area were determined, the solder bond would be sufficient to fulfill NASA soldering requirements.

As each printed circuit board was completed, it was subjected to a comprehensive static test to ensure that no damage occurred to the board or its components during the assembly. At the completion of the board test, the boards were inserted into the wire harness connectors contained in the chassis to perform the system functional test with the aid of the BTE. The functional test of the boards, individually as well as combined within the system, uncovered malfunctions for which corrective action was initiated. The details of the malfunctions and new recommendations are contained in the main body of this report. Prior to delivery, the engineering model was subjected to a thermal cycle test which covered the range from minus 10°C to plus 60°C. The results of this testing are contained in Section 4. As it was stated before, the acceptance test which constituted delivery was performed on 1 April 1966 at the CalComp facility. On 5 April 1966, the engineering model was presented to the NASA technical officer at the Goddard Space Flight Center. Power and input signals were applied, and the Engineering Model MRIR Telemetry Unit responded by presenting the correct data.

From the start of the contract to the hardware delivery of the Engineering Model MRIR Telemetry Unit, the total time frame for the design review, fabrication, assembly, and test of the telemetry unit was five months and one day.

### 1.3 ENGINEERING MODEL TELEMETRY UNIT GENERAL DESCRIPTION

The NIMBUS "B" MRIR Telemetry Unit interfaces with the MRIR Radiometer Electronics Unit to convert analog data to a serialized digital format. The logic circuitry within the MRIR Telemetry Unit samples in sequence each of five radiometer output channels. The analog information is gated to an Analog-to-Digital (A/D) Converter Unit where 34.7 A/D conversions per second are performed on each channel input. The A/D conversion is performed with an accuracy of 1 part in 256 (8 bit accuracy).

The output of the A/D Converter is formatted with a frame synchronization word to produce a 28.8 millisecond frame length. The serial bit-stream frame consists of one 8-bit frame synchronization word (10111000) and five 8-bit digitized conversions of the analog radiometer data (one word for each of the five channels). The formatted data is transmitted in a split-phase waveform to a satellite digital recorder at a 1.66-kc bit rate (208 cps data word rate). The least significant bit for each word is transmitted first.



#### 1.4 BENCH TEST EQUIPMENT GENERAL DESCRIPTION

The MRIR Telemetry Unit Digital Subsystem Bench Test Equipment is designed to facilitate the functional testing of the Engineering Model MRIR Telemetry Unit. The Bench Test Equipment generates the clock frequencies, analog voltages, and primary power required by the telemetry unit. By routing all interface signals through the test point panel, an evaluation of the various input/output signals can be made. The primary output of the telemetry unit subsystem, a split-phase code modulated signal, is demodulated and made available as a visual display.

Additional features, such as current monitoring facilities, incremental voltage sources, and dummy loads are contained in the test equipment, minimizing the accessory equipment required for a thorough test.

The digital electronics contained in the test equipment is mechanized from basic modules for ease of maintenance and replacement. To aid in maintaining the test equipment, miscellaneous remote controls and indicators are brought to the front panel of the electronics drawer.

The d-c voltages required to operate both the test equipment and the unit under test are provided by modular power supplies housed in the test console.

## SECTION 2

## ELECTRONIC REVIEW

2.1 PRINTED CIRCUIT BOARDS

The final design of the MRIR Telemetry Unit contains seven (7) printed circuit boards (PCB's). Five of the PCB's contain the electronics to initiate and perform the function for converting the analog input information into a digital format. The remaining two PCB's provide the necessary secondary power levels which are generated from a primary input voltage source of a nominal minus 24.5 volts. A brief description of each module and its function is presented below.

## a. Analog Input - 25-kc Generator

This board contains six MOS-FET devices (only five are used) which gate the analog information to the A/D Converter. A five flip-flop ring counter provides the commutating control. In addition, this board generates a 25-kc clock signal by using three flip-flops to divide the 200-kc input by eight.

b. A/D Converter

This board contains the precision voltage supply, the comparator amplifier, constant current sources, transistor switches, and a precision resistor-ladder network to accomplish the analog-to-digital conversion.

c. A/D Data Control

This board contains two 8-flip-flop registers. One register retains the data after the A/D conversion. The other register provides the control signal to successively turn on each current source. Depending on whether the analog voltage is greater than or less than the voltage generated by the ladder network, will determine whether a selected current source should be left on or turned off. This module also contains the Frame Sync Inhibit logic which changes the least significant bit to a "one" if analog data is converted to have the same bit pattern as the Frame Sync word.

d. Encode - Timing Generator

This board contains nine flip-flops which are used to provide timing control. Six flip-flops are used to divide a 10-kc input signal to 1.66 kc (one bit time) and 208 cps (one word time). A transfer pulse is generated to gate the converted information from the data register

on the A/D Data Control board to an output data shift register on the Frame Sync-Data Output board. In addition to the transfer pulse, a second timing pulse (ENCODE pulse) is generated. The ENCODE pulse clears the A/D data register, resets the A/D shift register, and starts the A/D conversion of new input data.

e. Frame Sync - Data Output

This board generates the Frame Sync word (10111000) every sixth word time. The function of the Frame Sync word is to provide a basis for synchronization when decommutating the telemetry data transmitted to a ground station. As was mentioned before, an 8-bit flip-flop shift register is contained on this board to provide the serial data output to two redundant data output buffer drivers. The data is transmitted in a split-phase waveform as shown in Figure 2-1.

f. DC/DC Converter No. 1

This board is one of two power supply boards which provides the secondary voltage levels. These levels are +3.2v, +6v, -6v, -12v, and -18v. Contained on this board are the primary power relay, flux oscillator, power transformer, and secondary voltage diode rectifiers. The DC/DC No. 1 board was designed so that all oscillating signals would be confined on this board and not be coupled into the wiring harness by sending the oscillating signals to another board for conditioning.

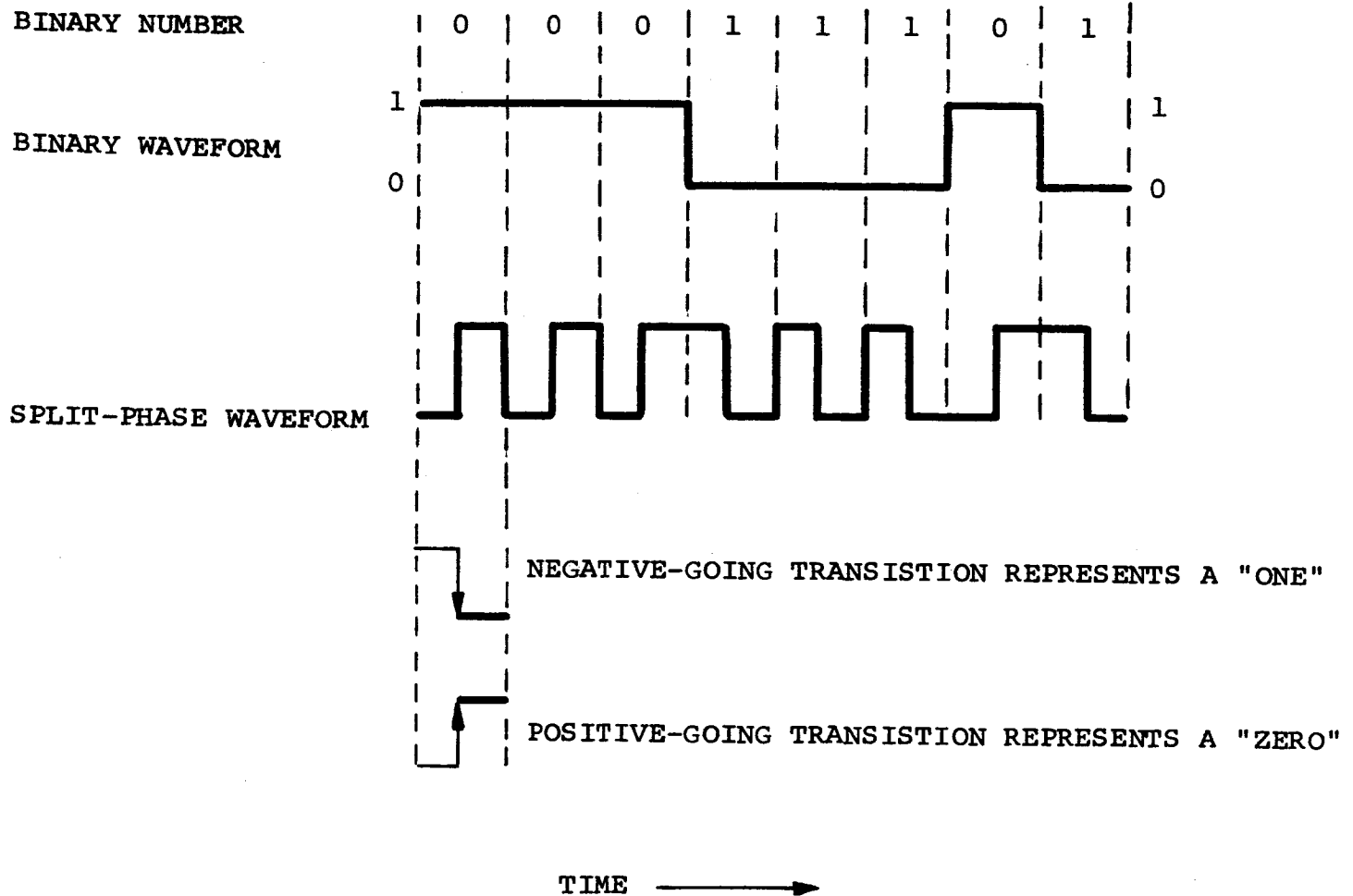


FIGURE 2-1  
Split-Phase Waveform

## g. DC/DC Converter No. 2

The second half of the two power supply boards contains the input filter network, voltage regulator, secondary level output filters, and the telemetry point circuits.

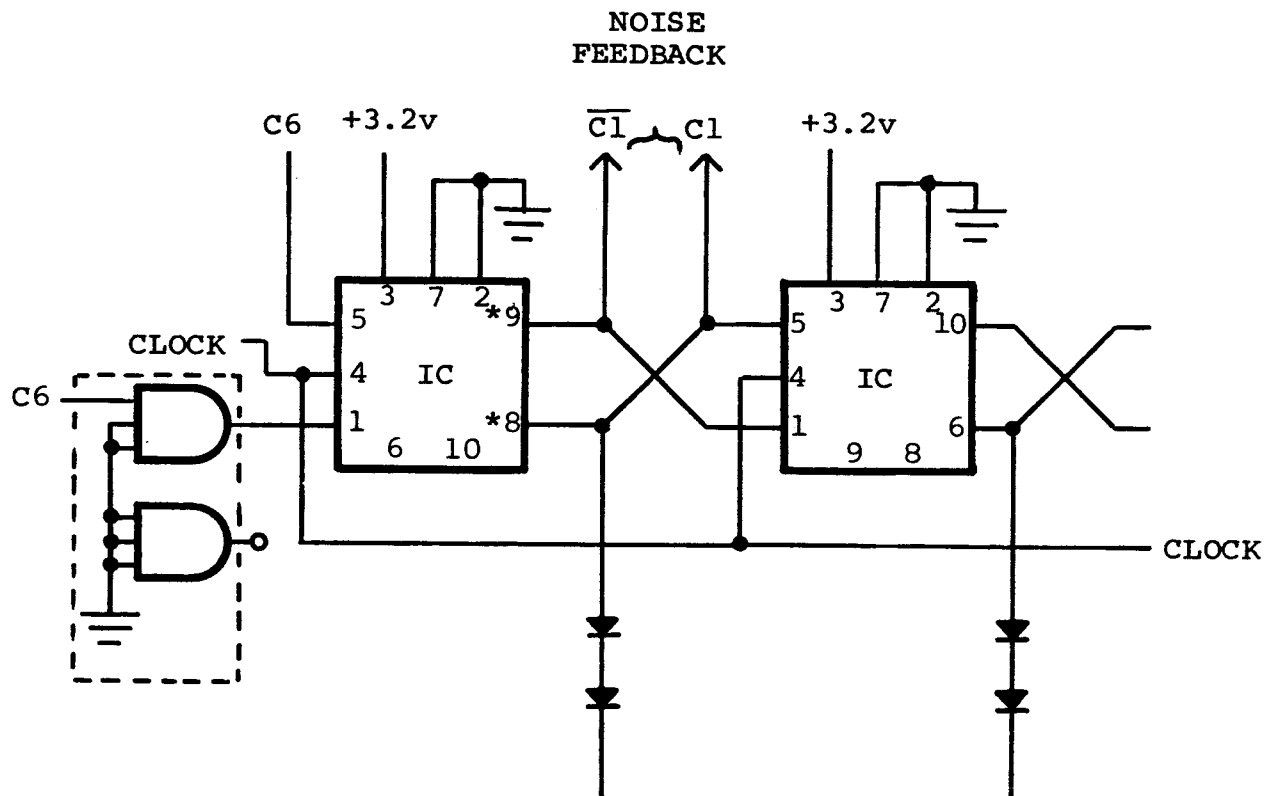
Test equipment to test the PCB's on an individual basis was designed and fabricated. To perform as complete a test as possible on each PCB, functional test specifications were generated for each PCB with the exception of the two power supply boards. These two boards are tested as a unit; therefore, one functional test specification covers both boards.

While performing the initial functional test on the PCB's, several problems were uncovered. The necessary action to solve these problems was initiated and the solutions have been implemented. The malfunctions spoken of here are the types which required printed circuit board modifications and drawing changes. Other discrepancies which have been found are of such a minor nature that they will not be discussed. These discrepancies involved wrong value components, failed parts, term exits on a pin other than noted on the schematic, etc. The intent here is to review each PCB type and comment on it. The electrical schematics and assembly drawings for all PCB's are found in Appendix A.

### 2.1.1 ANALOG INPUT - 25-KC GENERATOR BOARD

Of the seven PCB's in the MRIR Telemetry Unit, the Analog Input board presented the most problems. The major problem was that noise feedback on the output of the first stage of the commutation ring counter was sufficient to SET the second stage 300 microseconds after it was RESET. The RESET should have been for a time duration of 4.8 milliseconds. The circuit showing the situation when the faulty operation occurred is shown in Figure 2-2. The solution to this problem for the engineering model is shown in Figure 2-3. The gate which was contained on the board, but unused, provided the isolation from the noise feedback on the "zero" side output, while the collector provided isolation on the "one" side output. The use of both the collector output and the emitter-follower output on the "one" output side is ordinarily not a good practice because base drive for the emitter-follower output is reduced. However, in this instance, the emitter-follower fan-out load is only eight. Its maximum fanout is fifteen. Since the emitter follower is driving half its capacity, the simultaneous use of the flip-flop collector output does not divert enough base drive to hamper the emitter-follower operation.

The second problem area on the Analog Input board was the transformer isolation input filter network for the 200-kc clock signal. This network as shown in Figure 2-4 provided too much attenuation on the input clock, and the reduced



\*Emitter-Follower Output\*

FIGURE 2-2

# First Stage Input Commutator (Pre-Functional Test Design)



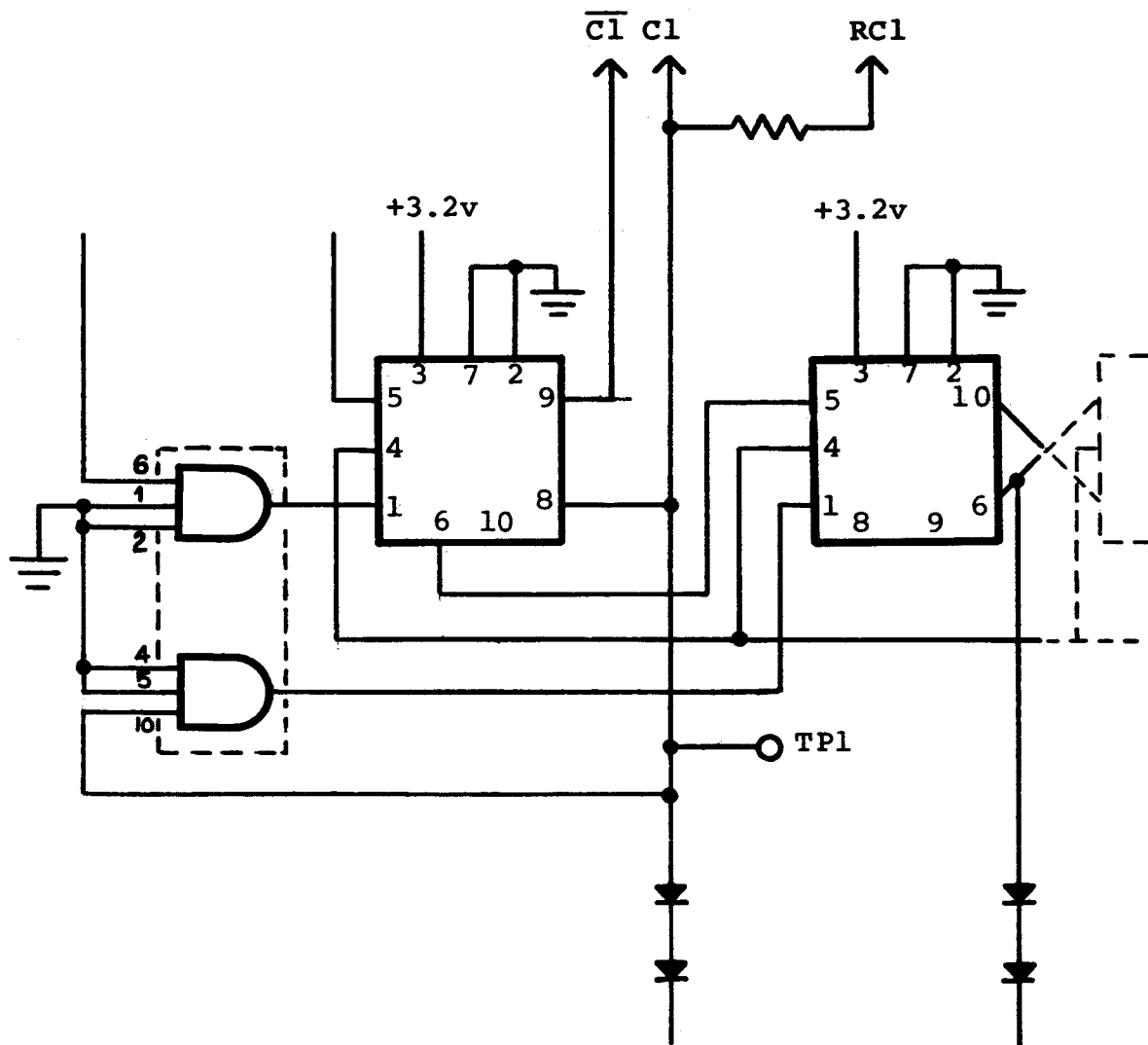


FIGURE 2-3

First Stage Input Commutator  
(Engineering Model Fix)

voltage was insufficient to drive the IC device. A review of the NIMBUS "C" MRIR design which had the same clock input requirement showed that this filter network was redesigned to that indicated in Figure 2-5. For the Engineering Model NIMBUS "B" MRIR Telemetry Unit, a compromise was made between the filter networks. The design used on the present MRIR engineering model is shown in Figure 2-6. However, for the subsequent prototype and flight model MRIR's, the filter network shown in Figure 2-5 will be included on the board.

#### 2.1.2 ANALOG/DIGITAL CONVERTER BOARD

The A/D board required some rework as a result of its functional test. Because of the accuracies involved, the A/D design is very sensitive. Extraneous noise was sufficient to cause the A/D Converter to operate erroneously. To remedy this situation, the board required additional components to eliminate the noise. One source of noise was the VLAD test point output term which is directly coupled through a 4700-ohm resistance to the comparator input circuit. This integrated circuit has a high impedance input and a very high gain. Any noise pickup on this line was coupled to the comparator input and amplified. To eliminate this action, the 4700-ohm resistor was replaced with a 100-picofarad capacitor tied to signal ground. The VLAD test point term has been eliminated and the noise is now filtered to ground.

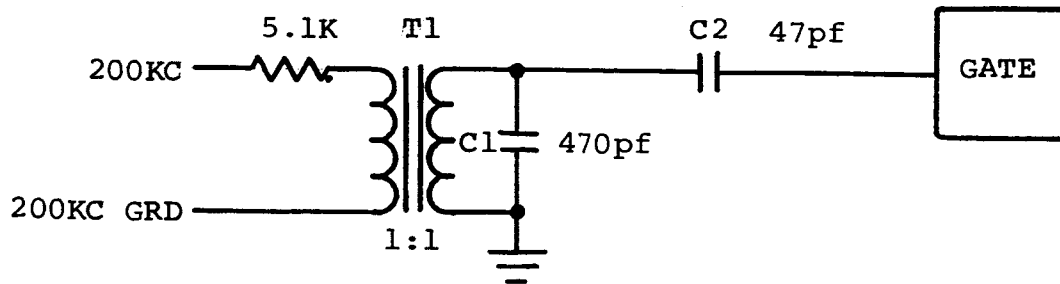
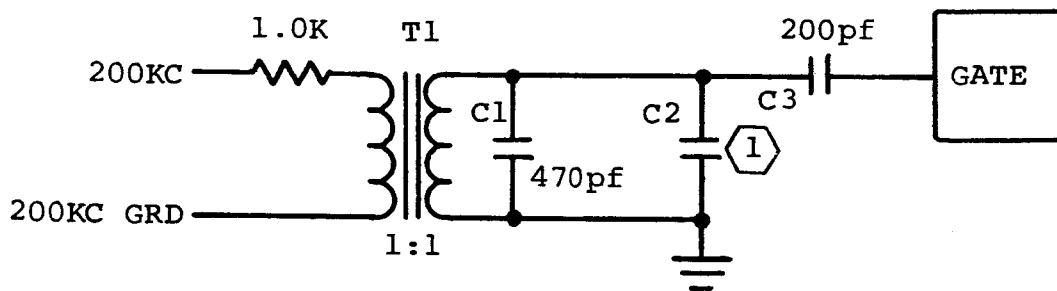


FIGURE 2-4

200KC Input Filter Pre-Functional Test Design



① Select

FIGURE 2-5

200KC Input Filter Prototype - Flight Model Design

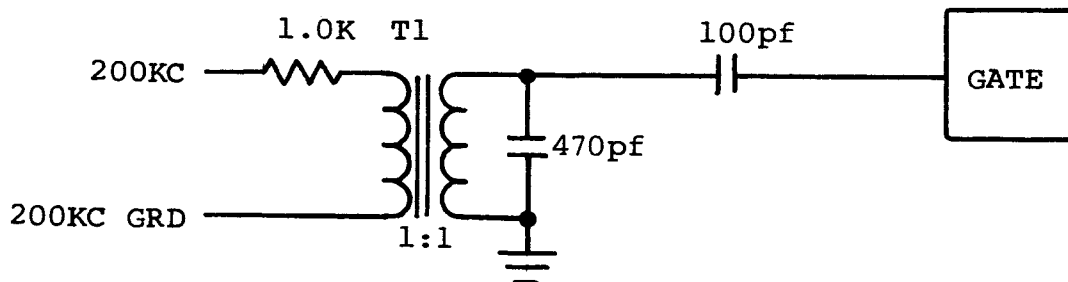


FIGURE 2-6

200KC Input Filter Engineering Model Design

The comparator amplifier required a frequency compensation capacitor between IC pins one and eight. When the A/D board was laid out, no provisions were provided for this compensation. Previous to the layout design, breadboard tests on this IC showed that no frequency compensation was required; however, when the board was fabricated and tested, the operational amplifier broke into a 1-megacycle oscillation when the null point between the actual data input and the ladder network output were approximately equal. A 10-picofarad capacitor was inserted between pins one and eight on the IC comparator amplifier to prevent this oscillation at the null point.

### 2.1.3 ANALOG/DIGITAL DATA CONTROL

The A/D Data Control logic board did not have any problems associated with it during the board test and the subsystem functional test. Prior to having the board fabricated, a logic error was found on the Frame Sync Inhibit logic. The logic was corrected, the artwork was updated, and the board was fabricated correctly. Figure 2-7 shows the logical representation for the correct mechanization. This mechanization will change the LSB of the data word to a "one" if the data word appears exactly as the Frame Sync word (10111000).

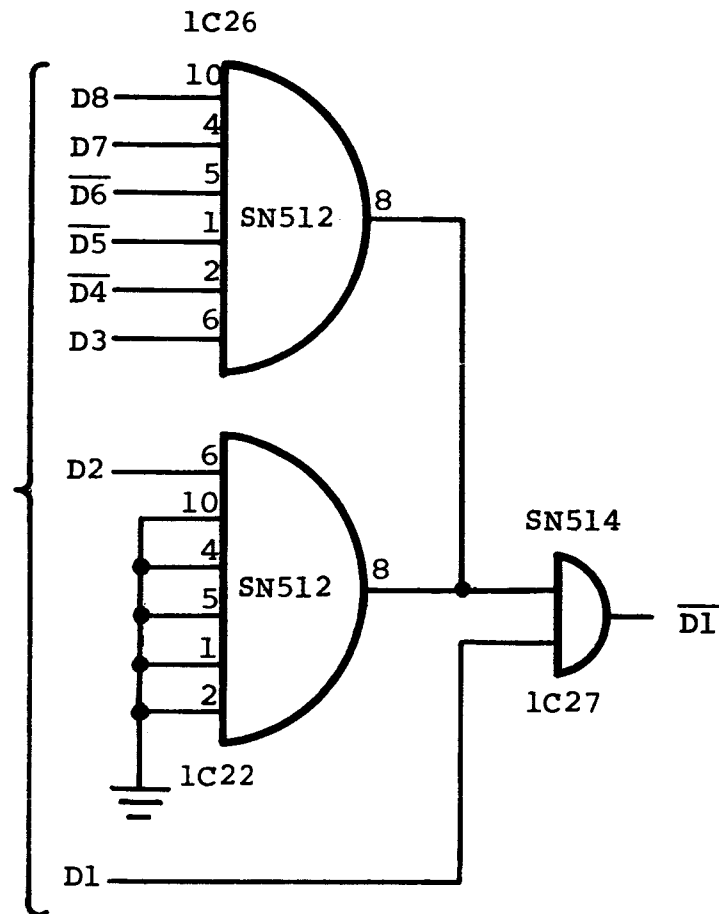


FIGURE 2-7

Frame Sync Inhibit Logic

#### 2.1.4 ENCODE-TIMING GENERATOR

The Encode-Timing Generator board did not require any changes.

#### 2.1.5 FRAME SYNC AND DATA OUTPUT

The Frame Sync and Data Output boards did not require any changes.

#### 2.1.6 DC/DC CONVERTER NOS. 1 AND 2

The two boards which provide the secondary voltage levels did not require any changes.

### 2.2 GROUNDING SCHEME AND VOLTAGE DISTRIBUTION

Figure 2-8 shows a signal flow diagram which contains the grounding scheme and voltage distribution. The grounding scheme in the MRIR was designed to avoid any ground loops. The power ground and signal grounds are in reality the same ground, but a difference is shown between the two. The power ground pertains to the DC/DC Converter boards, while the signal ground pertains to the other printed circuit boards. Chassis ground and telemetry ground are not internally tied to any point within the engineering model.

However, the telemetry points on the flight models will have the temperature telemetry point referenced to telemetry ground. The secondary power distribution is straightforward and presented no problems. The voltage distribution can be determined on the pin chart contained in Appendix D.

### 2.3 TELEMETRY POINTS

There are only three telemetry points contained within the Engineering Model MRIR Telemetry Unit. The points are used to monitor that the primary power relay has switched on command, that the minus 12 volt secondary level is maintaining regulation, and what the internal temperature is at the hottest point. A temperature sensitive component (Sensistor) is used to monitor the temperature. The output of the Sensistor as a function of voltage and temperature is shown in Figure 2-9. This curve can be used for calibration purposes. Appendix B gives the electrical information on the other two telemetry point outputs.

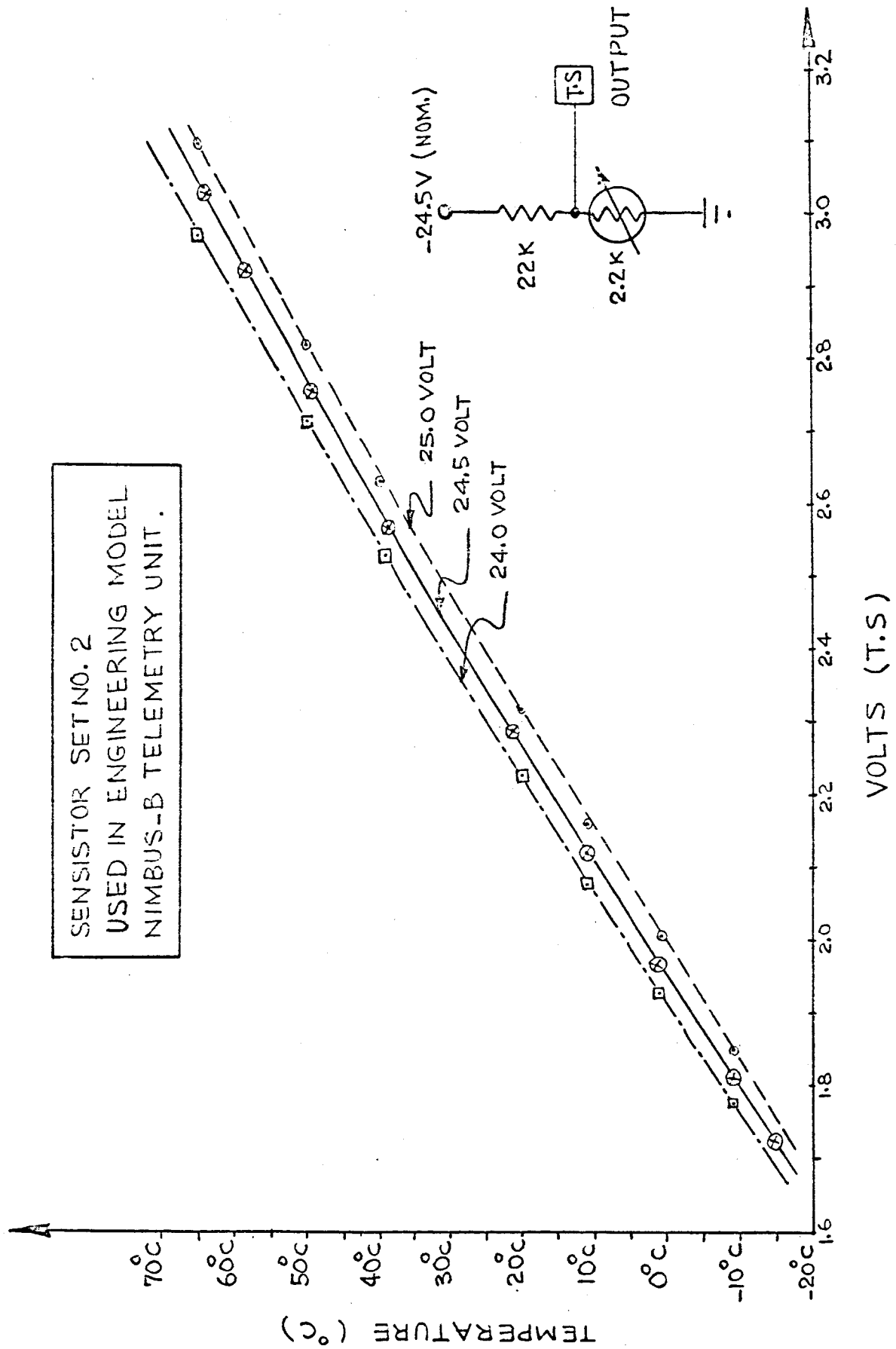


FIGURE 2-9  
TEMPERATURE TELEMETRY POINT



## 2.4 ELECTRICAL PRECAUTIONARY MEASURES

The use of MOS-FET devices has necessitated that extreme care be used in their handling. The devices can be easily damaged by static electricity or high positive voltage spikes. CalComp used precautionary measures during the board assembly as well as during functional test of the printed circuit board, and testing at the completed system level.

During the PCB assembly, the leads of the MOS devices were shorted together before, during, and after the assembly. A special 44-pin shorting plug was wired and attached to the board to tie all the input leads of the MOS devices to signal ground on that assembled module. At the system level, the analog inputs were routed to the J4 Bench Test connector so that a shorting plug (37-pin) provided protection when the MRIR telemetry was not connected. The procedure for system integration or connecting to the BTE is to install all cables to the other four connectors before removing the shorting plug to install the last cable, J4. The reverse procedure is used for cable removal.

## 2.5 ELECTRONIC DESIGN RECOMMENDATIONS

- a. On the Encode-Timing Generator board, a fix was made to isolate the emitter-follower outputs from the outputs going to the next stage of the

commutating ring counter. Instead of simultaneously using the collector output and emitter-follower output on the C1 flip-flop, it is recommended that a gate be added to eliminate the use of the collector output. The mechanization will then be as shown in Figure 2-10.

- b. During the course of performing the functional test at the board level and the completed system level, three failed MOS transistors have been encountered. The cause and nature of their failure cannot be explained because other areas of the board or system were under investigation and not the MOS devices themselves. When the attention was turned to the MOS transistors, the failures were detected. The task of removing a multilead TO-5 device from the PCB is a very tedious job and in most cases pads are lifted. In addition, there is the risk of causing a failure to the new device being installed. The MOS-FET's used in the MRIR Telemetry Unit contain two devices within the same TO-5 can. The failure of any one MOS device within the package requires that the package be replaced. The waste here is that one MOS device within the removed package is still good but cannot be used elsewhere. Since these MOS devices can be easily damaged in handling, it is recommended that one MOS device per package per analog input channel be used or

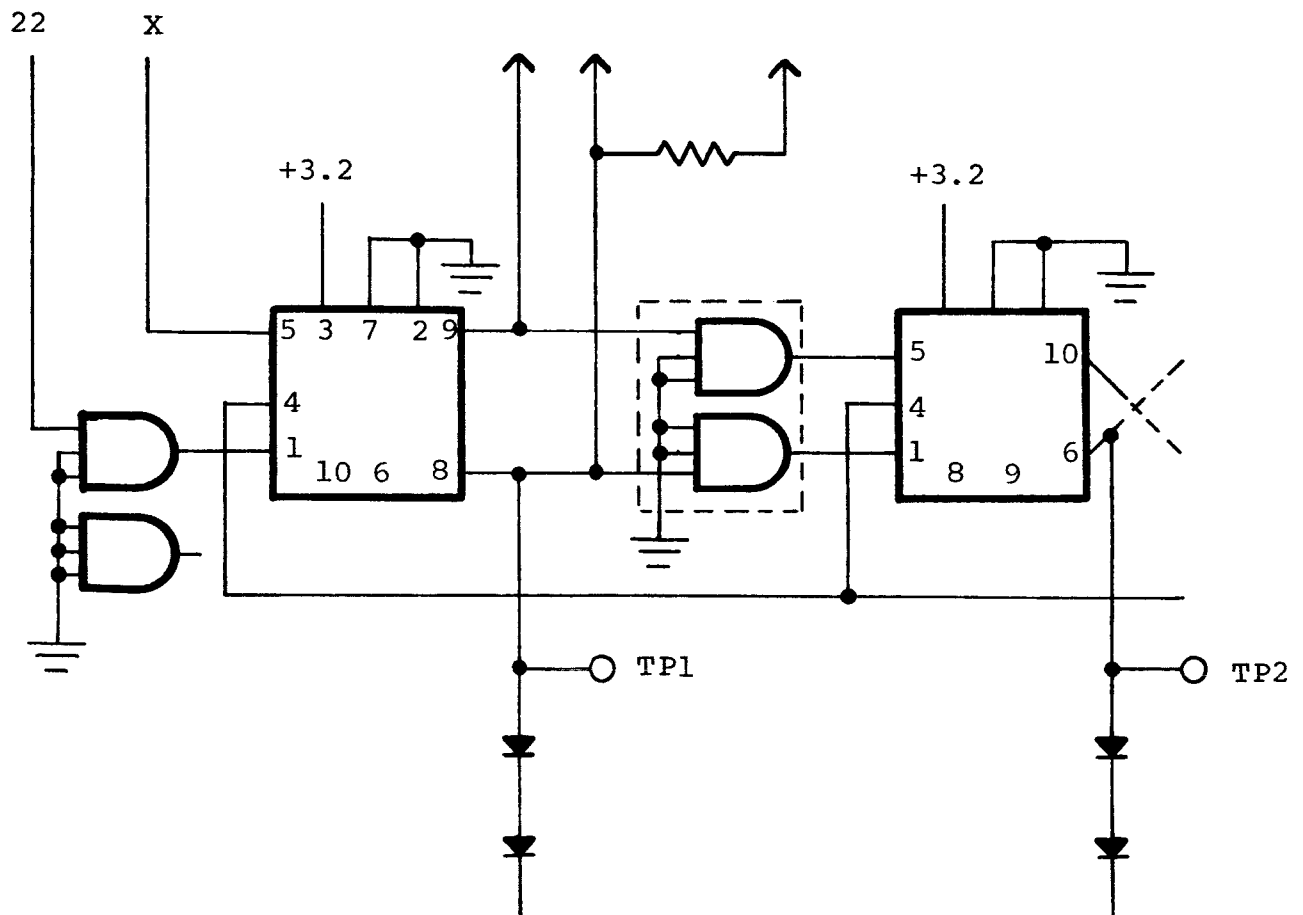
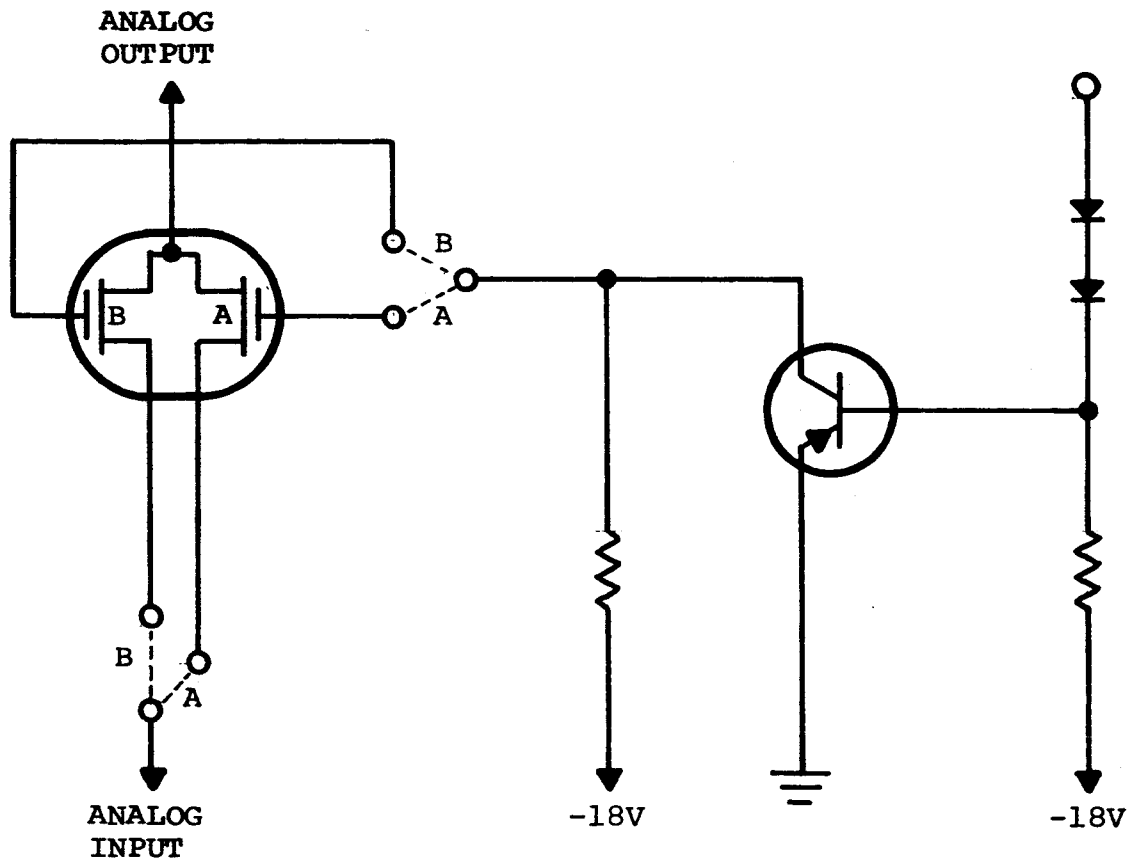


FIGURE 2-10

First Stage Input Commutator  
(Prototype - Flight Model Design Recommendation)

that the present two MOS devices per package be used except that the two devices be allocated for one channel only. For the latter recommendation, the five analog input channels would each have two MOS transistors (one package) each. The interconnection on the PCB could be done so that each channel input could be hardwired to use either of the two MOS devices available within the package. The mechanization for one channel input is shown in Figure 2-11. In the present layout, three MOS packages are used, but only five of the six available MOS-FET devices are wired into the circuit. The sixth is left hanging. The proposed scheme requires that only two additional T0-5 packages be added. This recommendation provides economy, saves repair time, and does not subject the PCB to damage which can be caused during repair.



Dotted lines represent shorting wires.

Wire B dotted lines for B MOS-FET.

Wire A dotted lines for A MOS-FET.

NOTE: Only one MOS-FET circuit is wired in at any one time.

FIGURE 2-11

Two MOS-FET Per Analog Input Channel

## SECTION 3

## MECHANICAL DESIGN

3.1 ENGINEERING MODEL MRIR TELEMETRY UNIT

## 3.1.1 PACKAGE LAYOUT

The layout of the Engineering Model MRIR Telemetry Unit was changed from the layout initially presented in the design study report to the layout shown in Figure 3-1. The Analog Input - 25-kc Generator board was placed as close as possible to the input/output connectors to keep the analog input lines short. Shields were placed between the analog input board and the input/output connectors to protect against crosstalk. The shield between the DC/DC Converter No. 1 board and the remaining logic modules was to isolate the logic modules from the flux oscillator circuit. The mechanical drawings containing the actual design of the Engineering Model MRIR Telemetry Unit are available in Appendix C.

No mechanical design problems were encountered when the engineering model MRIR was assembled. The machined magnesium parts were finished with the DOW 17 protective coating. All parts fit without modifications. The

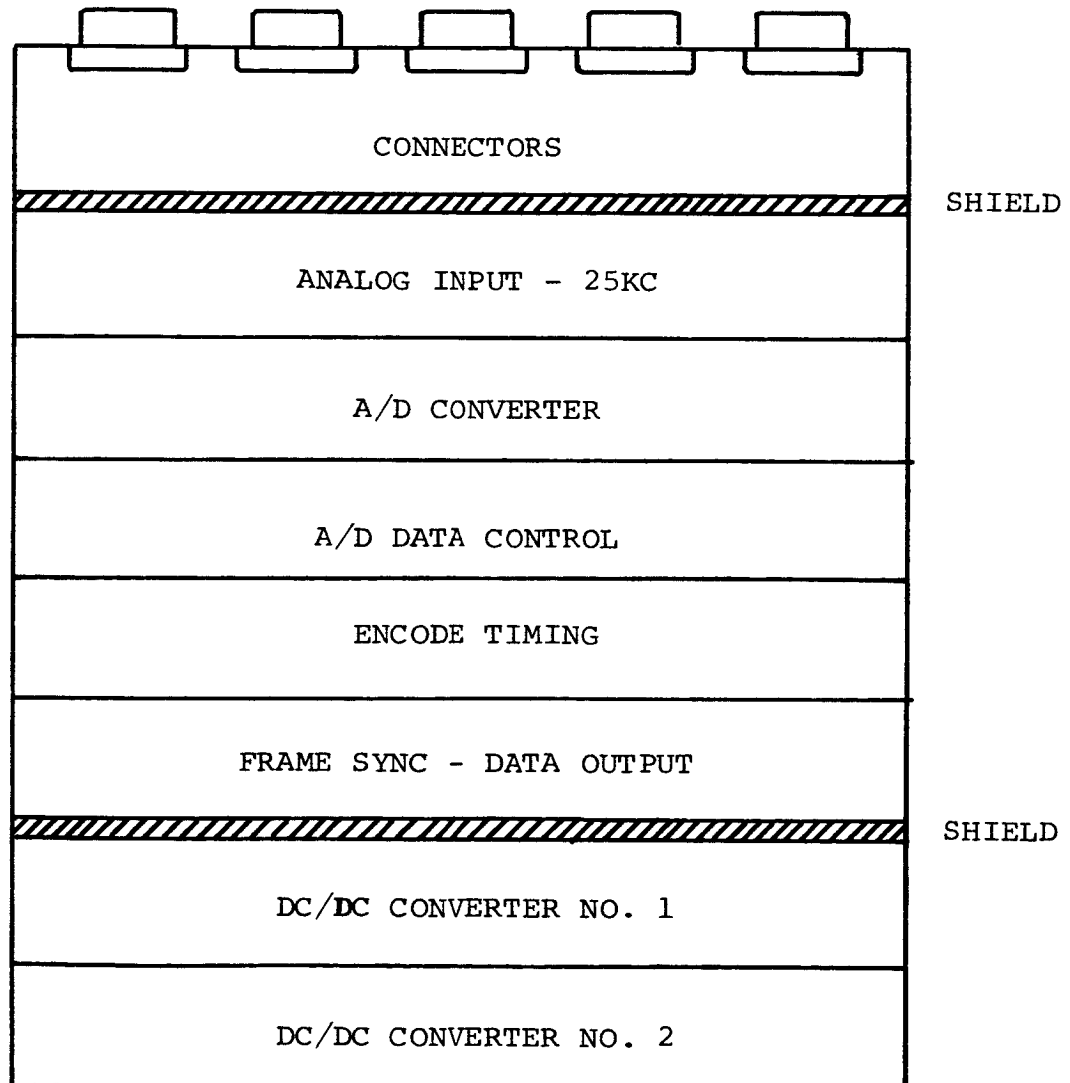


FIGURE 3-1  
Printed Circuit Board Allocation

mechanical design drawings pertaining to the chassis parts are complete. The final package size was 2 over 0 or 6 x 4 x 6.5 inches. The housing contained five input/output connectors which are labeled J1 through J5, and the type and function of each connector is indicated in Table 3-1. Each connector is different to prevent mismatching between cables and connectors.

Internal to the housing are seven 44-pin printed circuit board (PCB) connectors which are keyed to match a particular PCB. The PCB's contain slots corresponding to the keys.

### 3.1.2 PHYSICAL PARAMETERS

#### 3.1.2.1 Layout

The PCB layout of the Engineering Model MRIR Telemetry Unit is shown in Figure 3-1.

#### 3.1.2.2 Weight

The completed engineering model MRIR weighed 4.3 pounds (unpotted). This weight included the shorting plug on connector J4.

#### 3.1.2.3 Power Dissipation

The measured power dissipation of the engineering model



TABLE 3-1  
Input/Output Connectors

Connector	Number of Pins	Signals
J1	15-pin Plug	Power Input and Commands
J2	9-pin Socket	Output Signals
J3	15-pin Socket	Input Signals
J4	37-pin Socket	Telemetry and Bench Test Equipment Test Point
J5	9-pin Plug	Input Clock Signals

MRIR was 1.7 watts at minus 10°C. This figure represents the maximum power dissipation.

### 3.1.3 CENTER OF GRAVITY

The dimensions of measured center of gravity of the engineering model MRIR are shown in Figure 3-2.

### 3.1.4 MECHANICAL DESIGN RECOMMENDATIONS

The mechanical design is sufficient as it stands for the engineering model telemetry unit; therefore, prototype and flight models will be mechanically fabricated in the same manner as the engineering model.

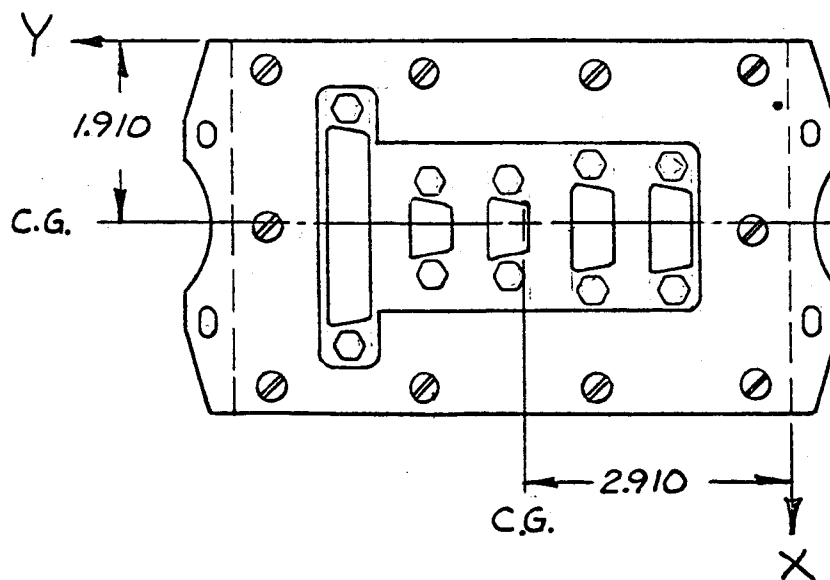
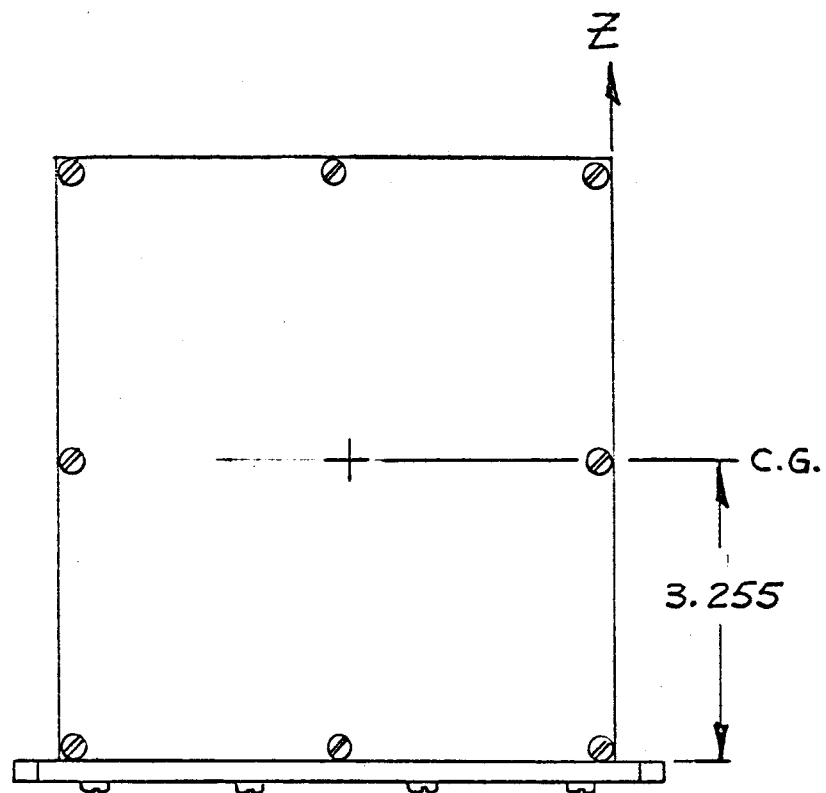


FIGURE 3-2

MRIR Telemetry Unit  
Engineering Model Center of Gravity

### 3.2 BENCH TEST EQUIPMENT

#### 3.2.1 PHYSICAL DESCRIPTION

The MRIR Telemetry Unit Bench Test Equipment is housed in two single bay racks. One rack, called the display console, houses the power supply drawer, test point panel, data display drawer, and a console blower. See Figure 3-3. The other rack, the auxiliary console, houses the remaining commercial test equipment, which includes a Tektronix RM45A oscilloscope, a Non-Linear Systems Model 484A digital voltmeter, and an Exact Electronics Model 250 function generator. In addition to a console blower, the latter bay is equipped with a loose equipment drawer and a writing surface. This unit is shown in Figure 3-4. A more comprehensive description can be obtained from the Bench Test Equipment Document D0106-004 entitled "Maintenance Manual for MRIR-PCM Bench Test Equipment, NIMBUS B," dated 24 March 1966.

Convenience outlets are available at the power supply drawer and the rear of the auxiliary console. Both consoles are designed to be operated from single-phase, 115-vac power. The display console is protected by a 10-ampere circuit breaker in the a-c line, with a 15-ampere breaker protecting the auxiliary console. In addition, the d-c power supplies are protected by a line fuse.

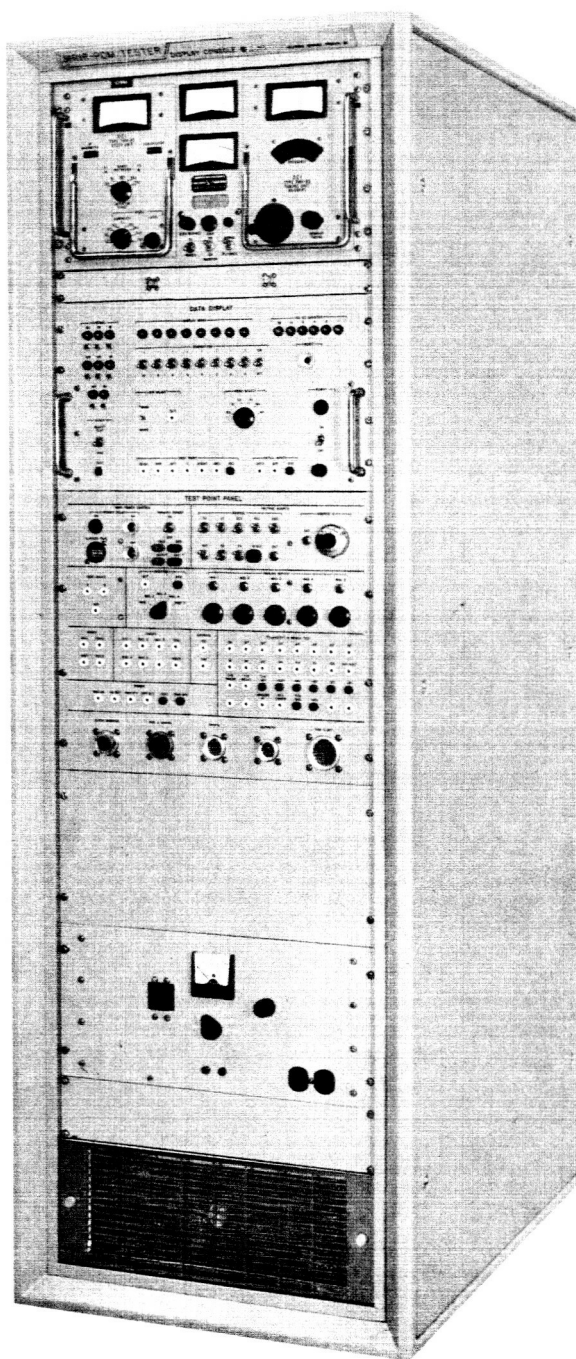


FIGURE 3-3  
Display Console

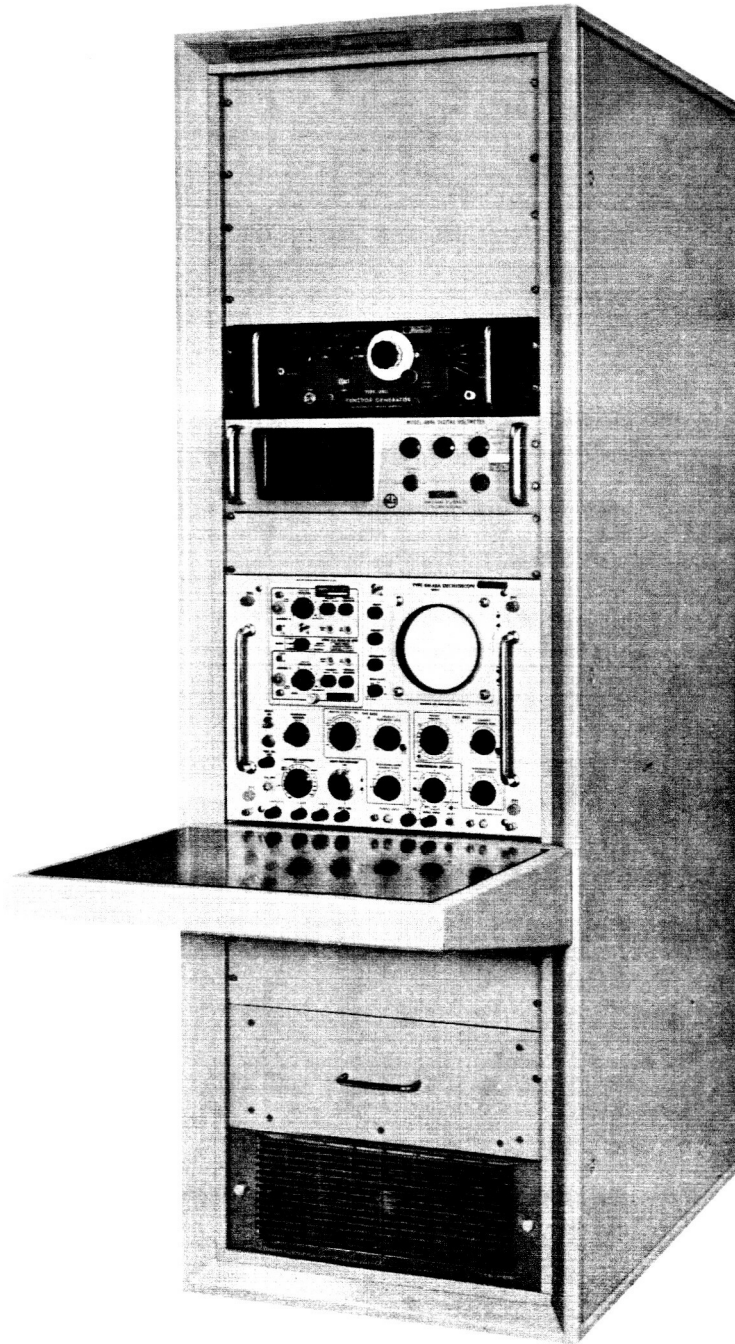


FIGURE 3-4  
Auxiliary Console

## SECTION 4

## SYSTEM TEST AND OPERATION

4.1 SYSTEM TEMPERATURE CYCLE TEST

The engineering model was placed into a temperature controlled oven to test the effects of the unit at +60°C, and at -10°C. The results of each test on a per channel basis are contained in Tables 4-1, 4-2, 4-3, and 4-4. In all cases, the MRIR unit was allowed to temperature soak (no applied power) for approximately forty-five minutes. The internal temperature of the unit was determined by monitoring the Sensistor.

4.2 MRIR TELEMETRY UNIT INTERFACE

The interface list for the Engineering Model MRIR Telemetry Unit is contained in Appendix B. The list provides the terms on each connector pin plus the equivalent voltages and impedances on those pins which originate or terminate on the telemetry unit.

### 4.3 MRIR TELEMETRY TIMING DIAGRAM

A timing diagram showing the relationship among the logic signals within the MRIR Telemetry Unit is presented in Figure 4-1 on page 4-6.

TABLE 4-1

MRIR Telemetry Unit Power Supply  
Temperature Test at +60°C Ambient

Secondary Voltage Levels	Primary Power Input		
	-24.0 $\pm$ 0.02v	-24.5 $\pm$ 0.02v	-25.0 $\pm$ 0.02v
+3.2 $\begin{smallmatrix} +0.23 \\ -0.10 \end{smallmatrix}$	+3.189	+3.189	+3.189
+6 $\pm$ 0.18	+6.128	+6.127	+6.128
-6 $\pm$ 0.18	-6.154	-6.154	-6.154
-12 $\pm$ 0.36	-12.25	-12.25	-12.25
-18 $\pm$ 0.54	-18.42	-18.42	-18.42



TABLE 4-2

MRIR Telemetry Unit Power Supply  
Temperature Test at  $-10^{\circ}\text{C}$  Ambient

Secondary Voltage Levels	Primary Power Input		
	$-23.5 \pm 0.02\text{v}$	$-24.5 \pm 0.02\text{v}$	$-25.5 \pm 0.02\text{v}$
+3.2 $\begin{smallmatrix} +0.23 \\ -0.10 \end{smallmatrix}$	+3.117	+3.117	+3.118
+6 $\pm 0.18$	+5.907	+5.907	+5.908
-6 $\pm 0.18$	-5.937	-5.938	-5.939
-12 $\pm 0.36$	-11.97	-11.97	-11.97
-18 $\pm 0.54$	-18.05	-18.05	-18.05

TABLE 4-3

MRIR Telemetry Unit Analog/Digital  
Conversion at +60°C Ambient Temperature  
(Nominal Voltage)

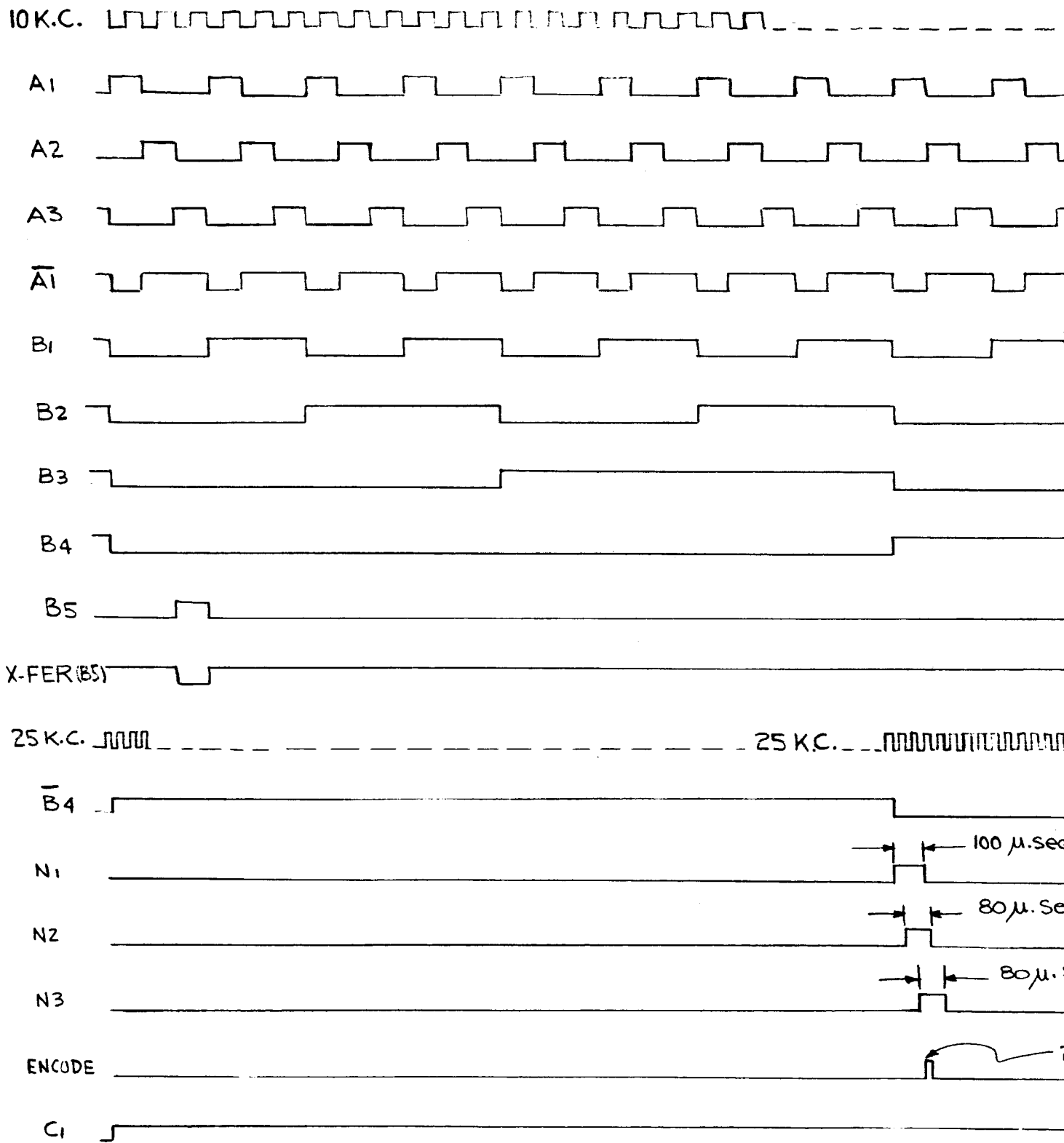
Bit	Channel				
	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
$2^0$ (25mv)	-18mv	-19mv	-20mv	-20mv	-20mv
$2^1$ (50mv)	-45	-45	-45	-45	-45
$2^2$ (100mv)	-94	-95	-95	-95	-95
$2^3$ (200mv)	-194	-195	-195	-196	-196
$2^4$ (400mv)	-396	-396	-396	-396	-396
$2^5$ (800mv)	-797	-797	-797	-797	-797
$2^6$ (1600mv)	-1596	-1596	-1596	-1596	-1596
$2^7$ (3200mv)	-3197	-3197	-3197	-3197	-3197
All Bits 6375mv	-6372	-6372	-6372	-6372	-6372

TABLE 4-4

MRIR Telemetry Unit Analog/Digital  
Conversion at  $-10^{\circ}\text{C}$  Ambient Temperature  
(Nominal Voltage)

Bit	Channel				
	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
$2^0$ -25mv	-19mv	-20mv	-20mv	-20mv	-20mv
$2^1$ -50mv	-44	-45	-45	-45	-45
$2^2$ -100mv	-94	-95	-95	-95	-95
$2^3$ -200mv	-194	-196	-196	-196	-196
$2^4$ -400mv	-396	-396	-396	-396	-396
$2^5$ -800mv	-796	-796	-796	-796	-796
$2^6$ -1600mv	-1596	-1596	-1596	-1596	-1596
$2^7$ -3200mv	-3197	-3197	-3196	-3196	-3196
All Bits -6375mv	-6372	-6372	-6372	-6372	-6372

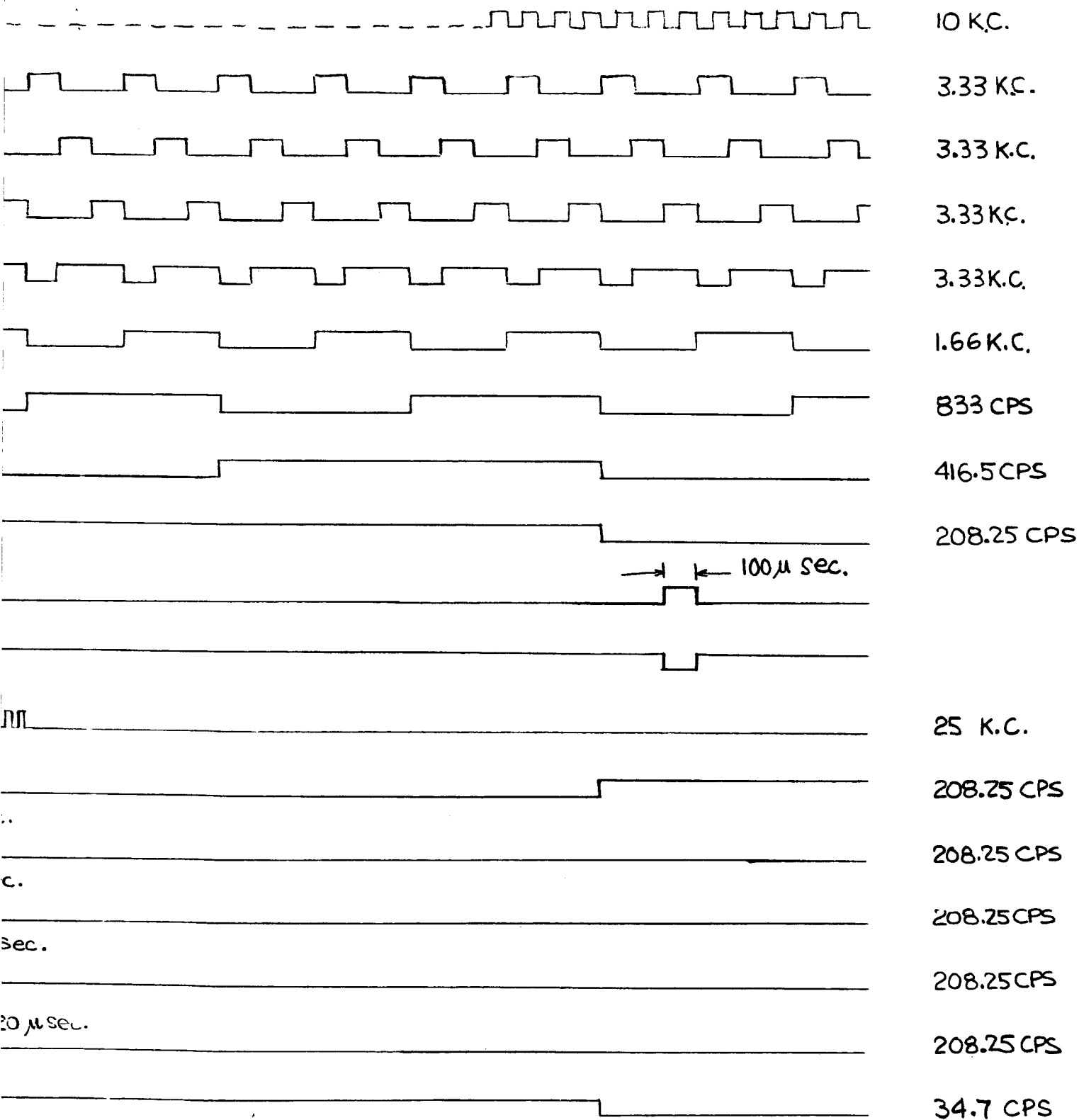
# TIMING CHART



FIGURE

4-6-1

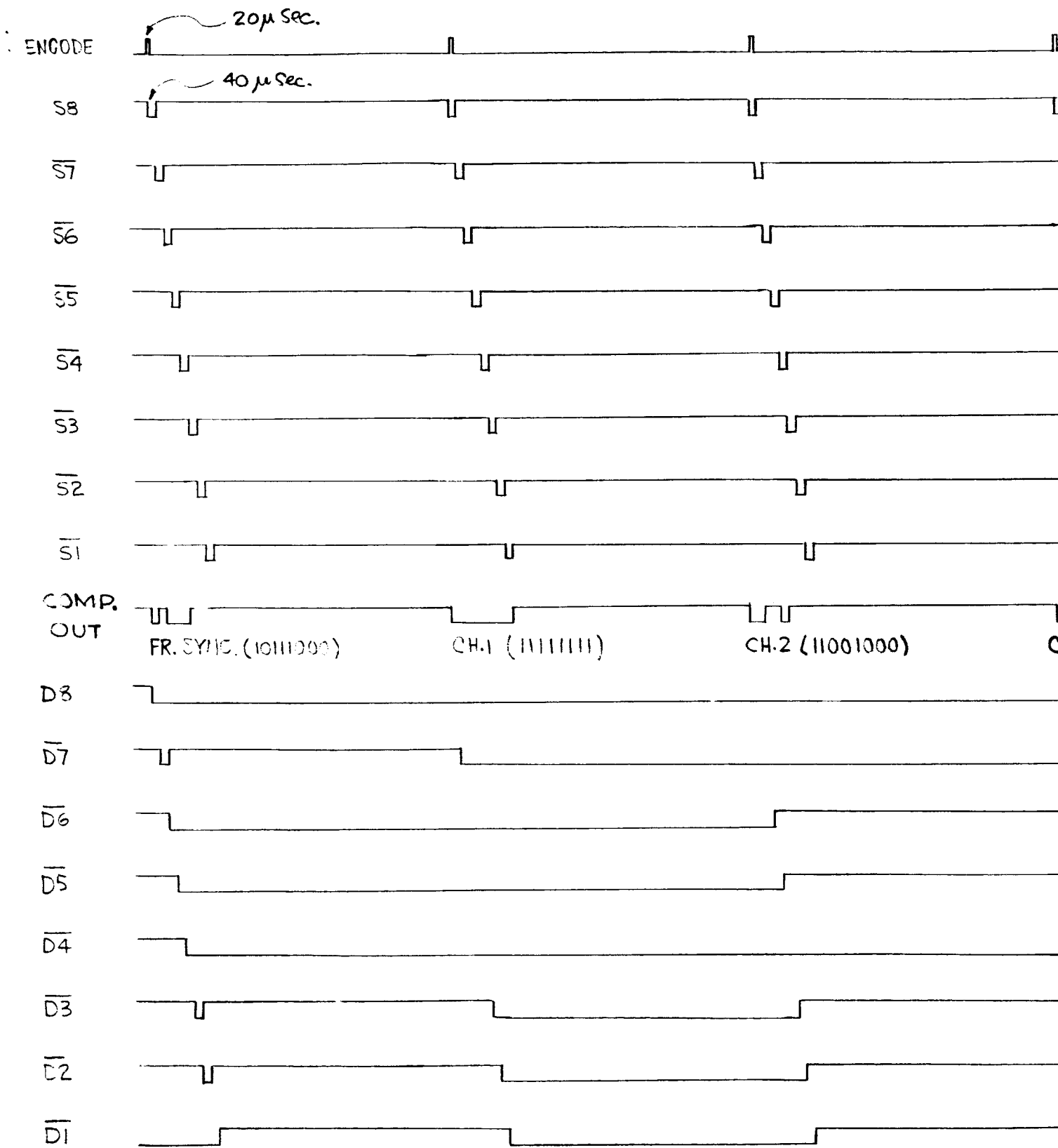
# T NIMBUS-B MRIR (TELMETRY UNIT)



4-1

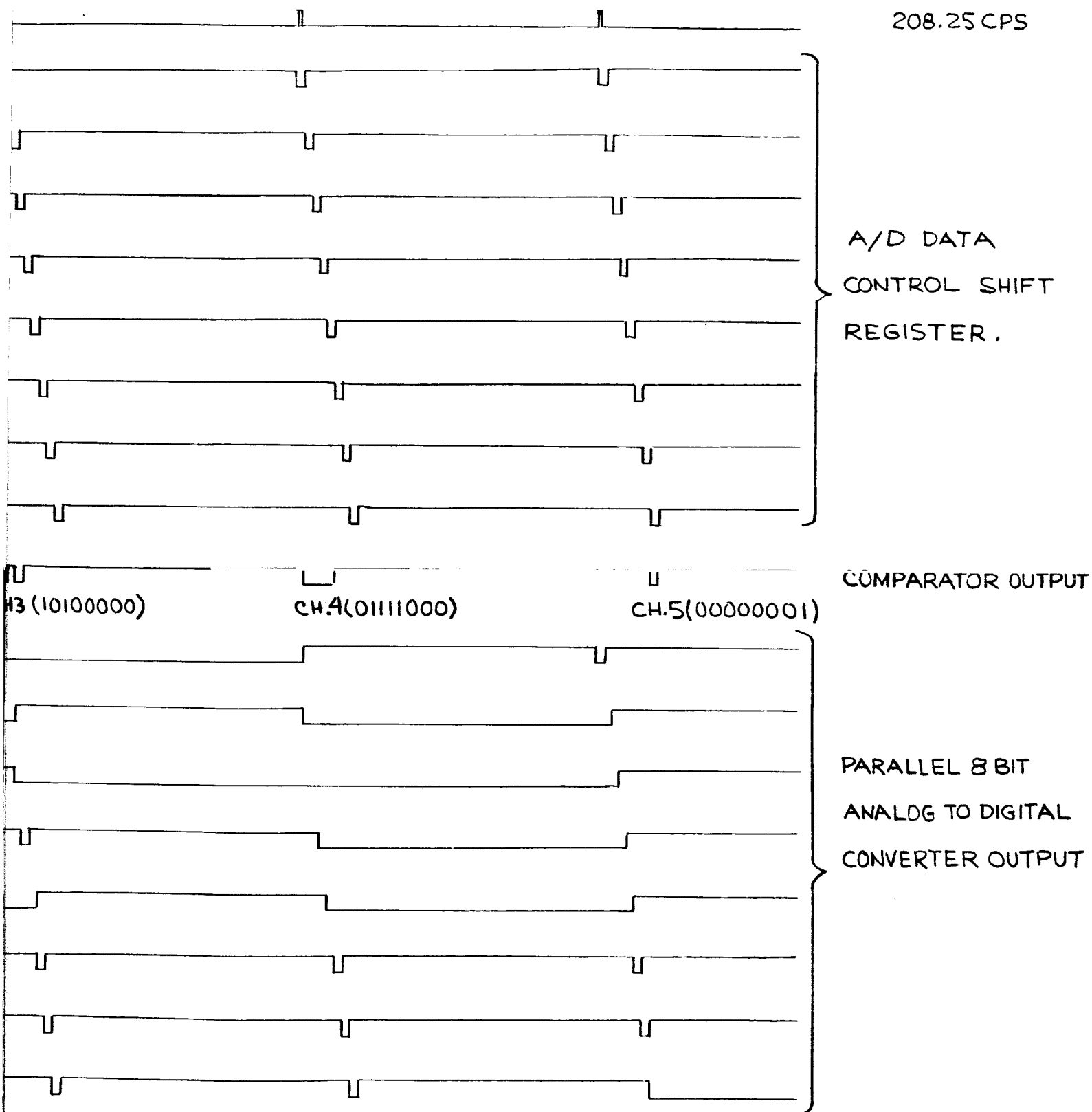
4-6-2

1 OF 3



NOTE :- CH1 = 0.375 VOLT, CH2 = 5.0 VOLT, CH

4-7-1



CH3 = 4.0 VOLT, CH4 = 3.0 VOLT, CH5 = 0.025 VOLT.

4-7-2

ENCLOS

20  $\mu$ sec.

B4

C1

C2

C3

C4

C5

C6

F

B1

$\overline{B1}$

TRO

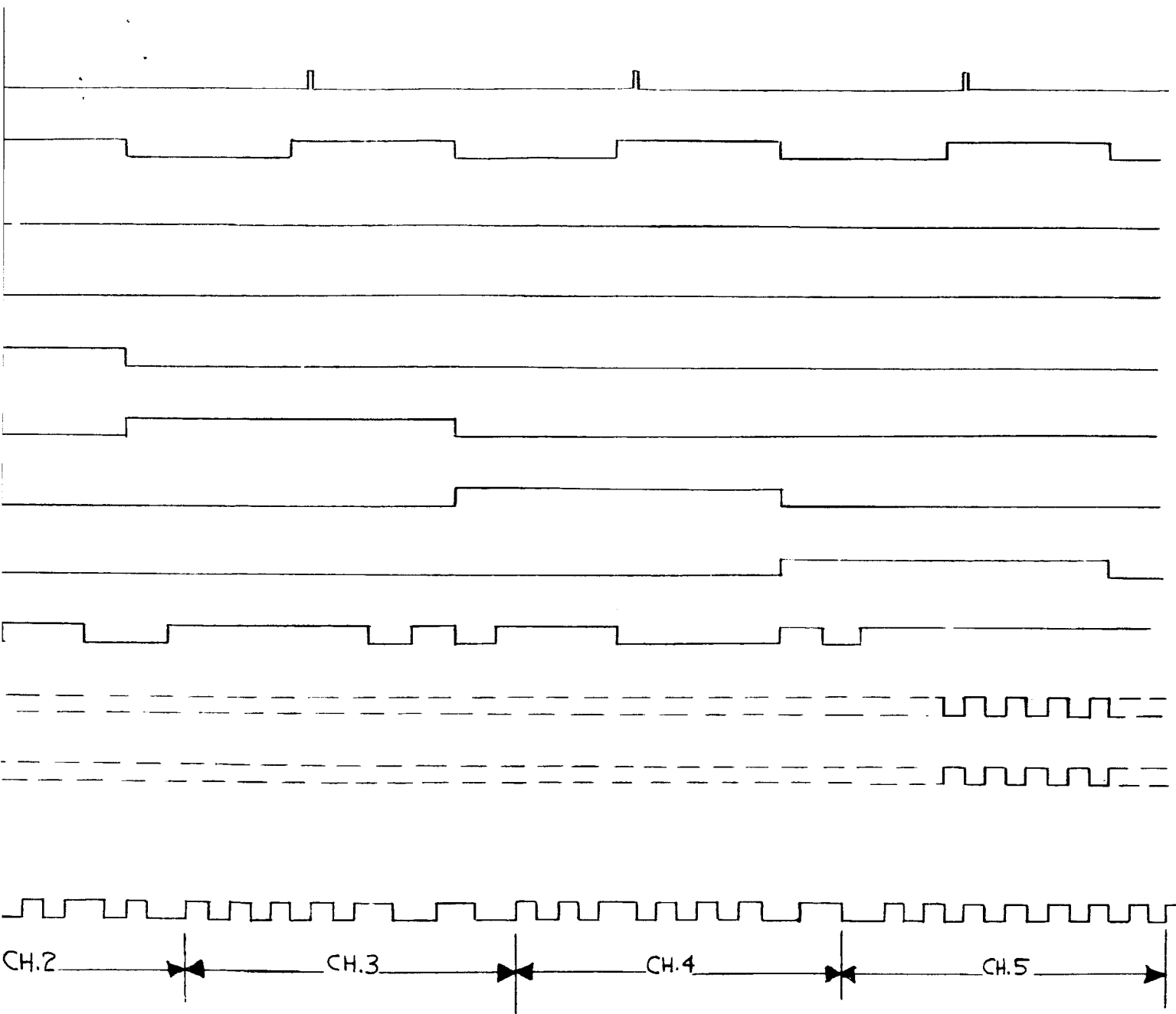
CH.5

FRAME

CH.1

4-8-1





F = SERIAL DATA OUTPUT

TRO = SPLIT PHASE SERIAL OUTPUT  
TO TAPE RECORDER.

4-8-2

#### 4.4 INTERCONNECTION DIAGRAM

Appendix D provides a combination wire list and inter-connecting diagram. The JXXX numbers associated with the connector terms indicate where the wire is going.

## SECTION 5

## NEW TECHNOLOGY

Throughout the performance of the contract NAS5-9699, a continual review of the work performed was conducted by a designated committee, including the Project Manager and the Patent Counsel. The committee met periodically to discuss all effort performed with a view to ascertaining reportable items disclosed in performance of the contract, both by the contractor and all subcontractors.

5.1 RESULTS OF CONTRACTOR'S REVIEW

The following are considered reportable items under the "New Technology" clause:

- a. Reportable Item: Analog-to-Digital Converter Circuit.

Invention Status: Not reasonably patentable.

Apparent Use: An analog-to-digital converter.

Description: The analog-to-digital converter for this contract is based almost entirely on the design submitted by NASA to the contractor. The contractor made some component changes

in incorporating some new integrated components which the contractor bought as off-the-shelf items from Fairchild Semiconductor Corporation. The design of the circuit was slightly different due to the requirements of the integrated components. The complete circuit is shown in this report as drawing No. D-10368-502.

- b. Reportable Item: Interface Buffer Circuit.  
Invention Status: Not reasonably patentable.  
Apparent Use: A data output buffer circuit.  
Description: The data output buffer circuit for the frame sync and data output is of standard design utilizing integrated circuit components. The circuit is based on the design submitted to the contractor by NASA. The circuit is shown in drawing No. 10354-502.

There were no subcontractors reportable under the "New Technology" clause.

## SECTION 6

### BIBLIOGRAPHY

The following documents are directly related to the design and development of the Engineering Model MRIR Telemetry Unit.

#### 6.1 TECHNICAL REPORTS AND MANUALS

- a. D0201-65/118 - 21 September 1965

A technical proposal for a Medium Resolution IR (MRIR) Experiment Engineering Model Digital Electronics Telemetry Unit for NIMBUS "B."

- b. D0301-013 - 31 December 1965

Reliability Assessment and Development Study Report on MRIR-PCM Subsystem.

- c. D0106-003 - 10 March 1966

Operator's Manual for MRIR-PCM Digital Subsystem Bench Test Equipment, NIMBUS "B."

- d. D0106-004 - 24 March 1966

Maintenance Manual for MRIR-PCM Bench Test Equipment, NIMBUS "B."

- e. 20101-01 - 23 November 1965  
Engineering Model MRIR Telemetry Unit Telecon Report.
- f. 20101-02 - 7 December 1965  
Engineering Model MRIR Telemetry Unit Telecon Report.
- g. 20101-03 - 9 December 1965  
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- h. 20101-04 - 14 December 1965  
Engineering Model MRIR Telemetry Unit DC/DC Converter Analysis.
- i. 20101-05 - 20 December 1965  
Engineering Model MRIR Telemetry Unit Telecon Report.
- j. 20101-07 - 5 January 1966  
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- k. 20101-08 - 11 January 1966  
Engineering Model MRIR Telemetry Unit Telecon Report.
- l. 20101-09 - 18 January 1966  
Engineering Model MRIR Telemetry Unit Telecon Report.

- m. 20101-010 - 19 January 1966  
Stresses Caused by Module Clamps.
- n. 20101-011 - 4 February 1966  
Engineering Model MRIR Telemetry Unit Telecon Report.
- o. 20101-014 - 22 March 1966  
Engineering Model MRIR Telemetry Unit Telecon Report.

6.2 MONTHLY PROGRESS REPORTS

- a. D0513-001 - 14 December 1965  
Monthly Progress Report No. 1 for MRIR-PCM Telemetry Unit, 1 November 1965 - 28 November 1965
- b. D0513-002 - 11 January 1966  
Monthly Progress Report No. 2 for MRIR-PCM Telemetry Unit, 29 November 1965 - 2 January 1966.
- c. D0513-003 - 8 February 1966  
Monthly Progress Report No. 3 for MRIR-PCM Telemetry Unit, 2 January 1966 - 31 January 1966.
- d. D0513-004 - 7 March 1966  
Monthly Progress Report No. 4 for MRIR-PCM Telemetry Unit, 1 February 1966 - 28 February 1966.
- e. D0513-005 - 14 April 1966  
Monthly Progress Report No. 5 for MRIR-PCM Telemetry Unit, 1 March 1966 - 31 March 1966.

6.3 FUNCTIONAL TEST SPECIFICATIONS

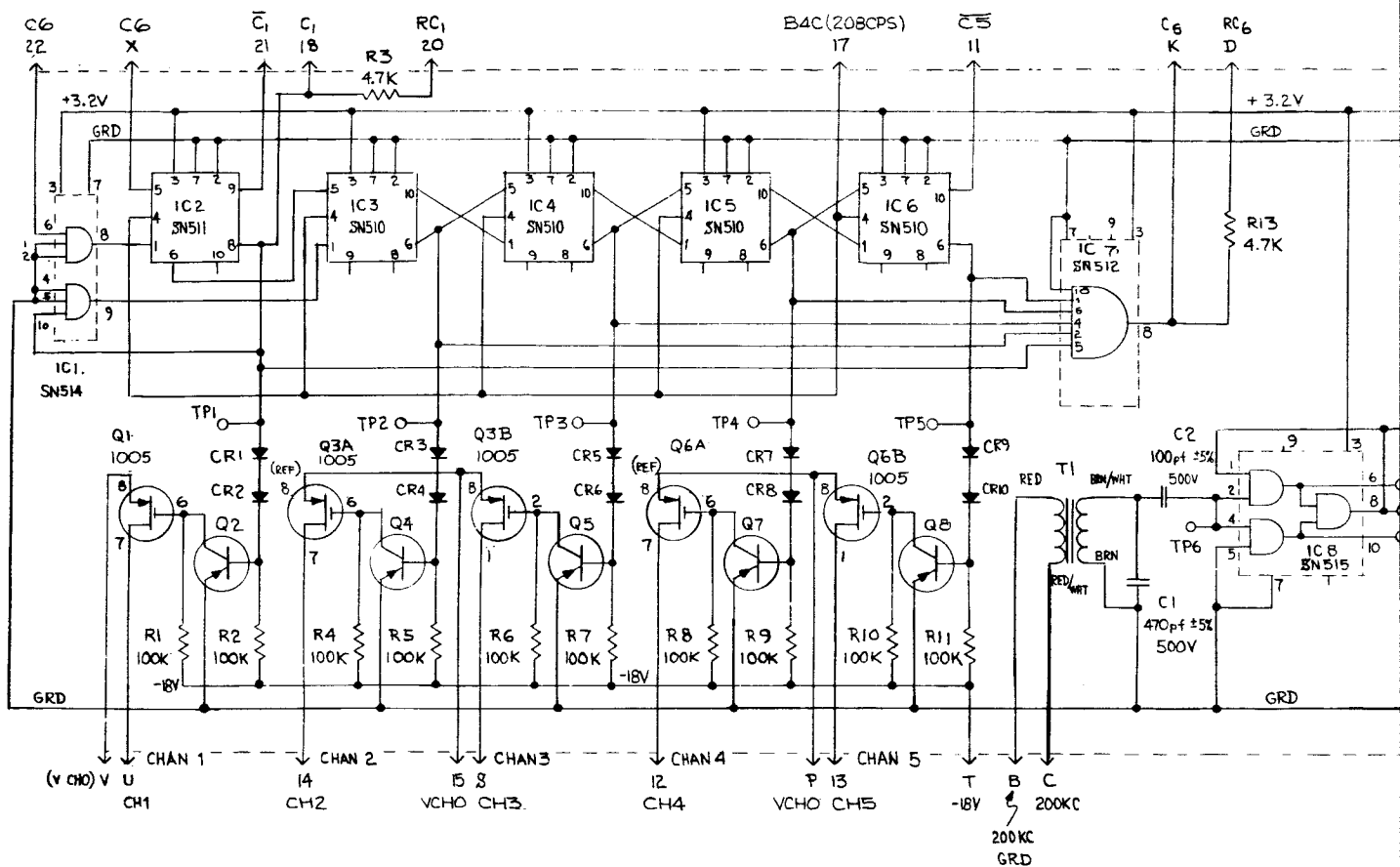
- a. A0205-101 - 29 April 1966  
Functional Test Specification for Analog Input  
and 25-KC Generator.
- b. A0205-102 - 5 May 1966  
Functional Test Specification for Analog-to-  
Digital Converter.
- c. A0205-103 - 29 April 1966  
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Digital Data Control.
- d. A0205-104 - 29 April 1966  
Functional Test Specification for Encode-  
Timing Generator.
- e. A0205-105 - 2 May 1966  
Functional Test Specification for Frame Sync  
and Data Output.
- f. A0205-106 - 10 May 1966  
Functional Test Specification for DC-to-DC  
Converter No. 1 and No. 2.
- g. A0201-019 - 10 March 1966  
Functional Test Specification for the MRIR-PCM  
Digital Subsystem, NIMBUS "B."



D0301-014

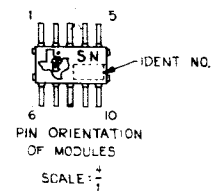
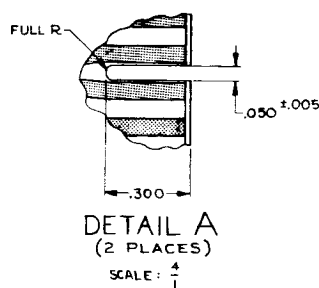
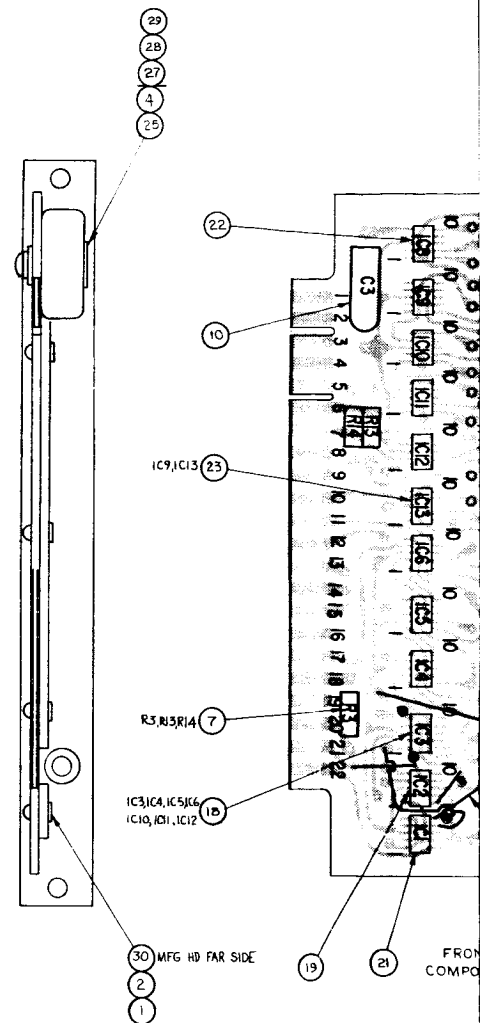
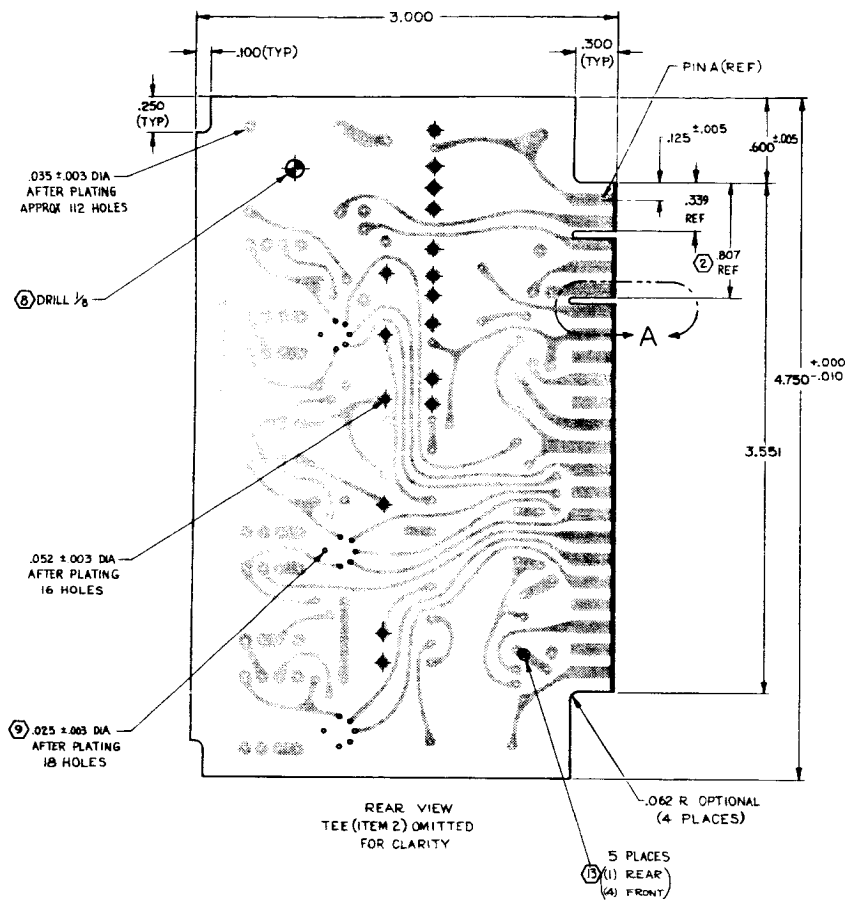
APPENDIX A

MRIR TELEMETRY UNIT  
ELECTRICAL SCHEMATICS  
AND  
PRINTED CIRCUIT BOARD ASSEMBLY DRAWINGS

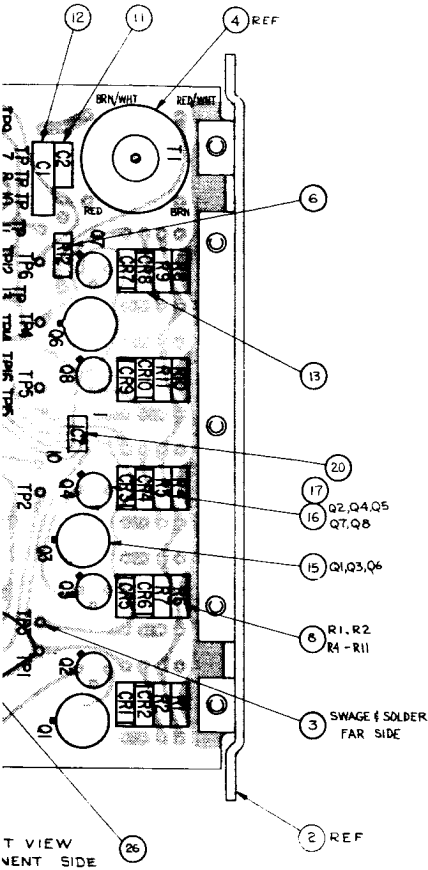


4. REF ASSY D  
 3. ALL RESIST  
 2. ALL DIODES  
 1. ALL TRANSI  
 NOTE: UNLESS C





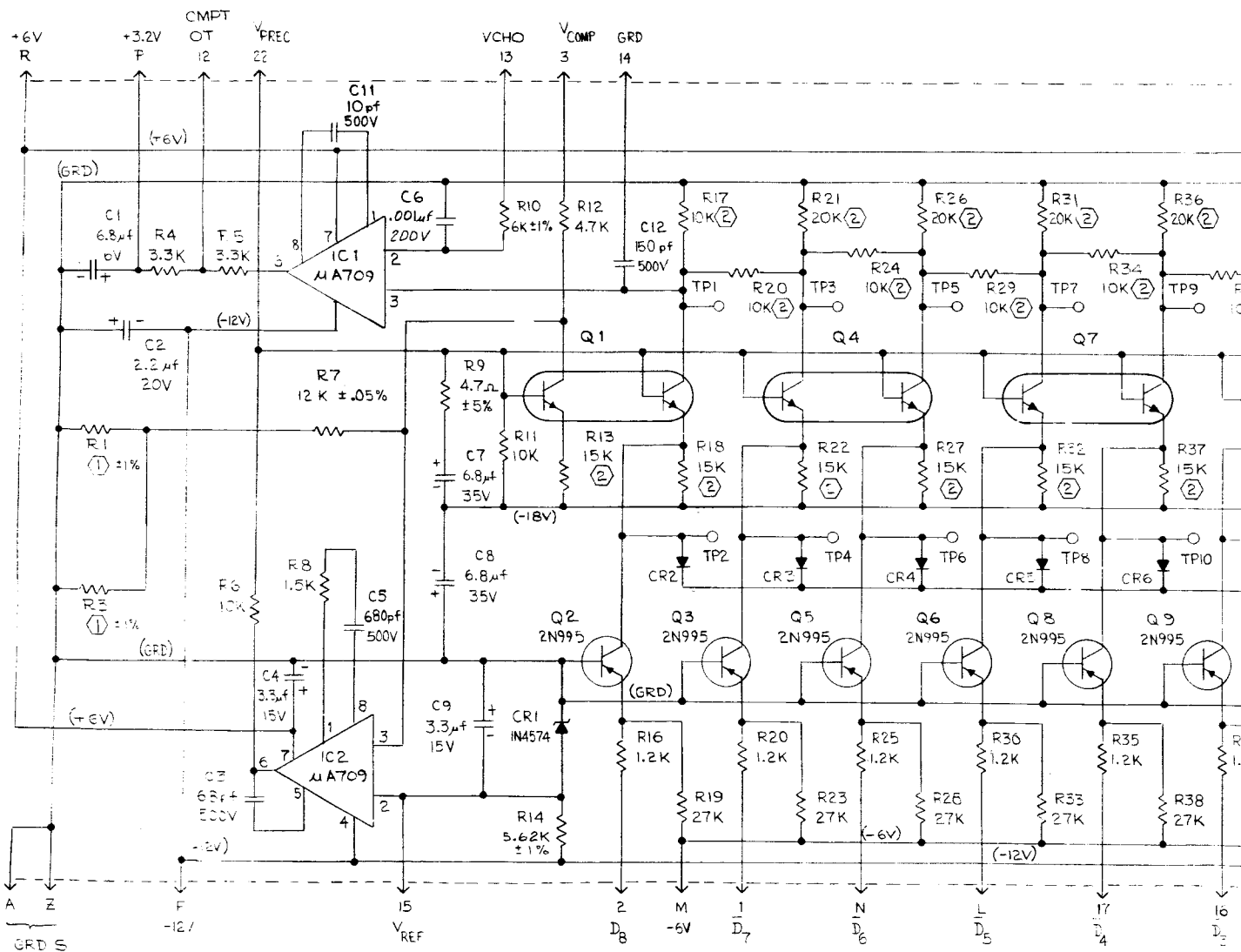
REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
		1 MAY BE REWORKED 2 CANNOT BE REWORKED 3 NONE	



- 13/22 CIRCUITRY TO BE CUT AT PLACES INDICATED BY ●
- 21 REA MAGNETIC WIRE CO INC, FORT WAYNE, IND
- 20 KIDWELL INC, VAN NUYS, CALIF
- 19 GENERAL ELECTRIC CO SEMICOND DIV, SYRACUSE, N.Y.
- 18 HOLES TO BE LANDLESS PER CCP SPEC A0105-007
- 17 DO NOT PLATE THRU
- 16 MODULAR ELECTRONICS, INGLEWOOD, CALIF
- 15 TEXAS INSTRUMENTS INC, DALLAS, TEXAS
- 14 GENERAL MICRO ELECTRONICS INC, SANTA CLARA, CALIF
- 13 KEMET DEPT UNION CARBIDE CORP, CLEVELAND, OHIO
- 12 CORNING GLASS WORKS, BRADFORD, PA
- 11 REF SCHEMATIC DWG NO. 10350-502
- 10 COMPONENT REF DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND DO NOT APPEAR ON ACTUAL PART.
- 9 KEY-SLOT DIMENSIONS ARE FOR REFERENCE ONLY, SLOT SHOULD BE CENTERED BETWEEN PINS AND MUST NOT TOUCH CIRCUITRY.
- 8 MATCH DRILL AND RIVET ITEMS 1 AND 2 USING JIG FIXTURE 11430-203
- 7 FABRICATE PER CCP SPEC A0105-007
- 6 SILK SCREEN USING SSM 10351-502-3
- 5 FABRICATE USING PCM 10351-502-3
- 4 EPOXY GLASS LAMINATE WITH 2 OZ COPPER BOTH SIDES, MIL-P-13949C, TYPE GE
- 3 PLATING:
- a - COPPER PLATE HOLES .001 MIN.
  - b - NICKEL PLATE HOLES AND CIRCUITRY .00050 MIN.
  - c - GOLD PLATE HOLES AND CIRCUITRY .000050 MIN.
- 2 CHAMFER CONNECTOR TIP .020 X .30" BOTH SIDES.
- 1 BOARD THICKNESS AT CONNECTOR TIP NOT TO EXCEED .065 ± .005
- NOTE: UNLESS OTHERWISE SPECIFIED

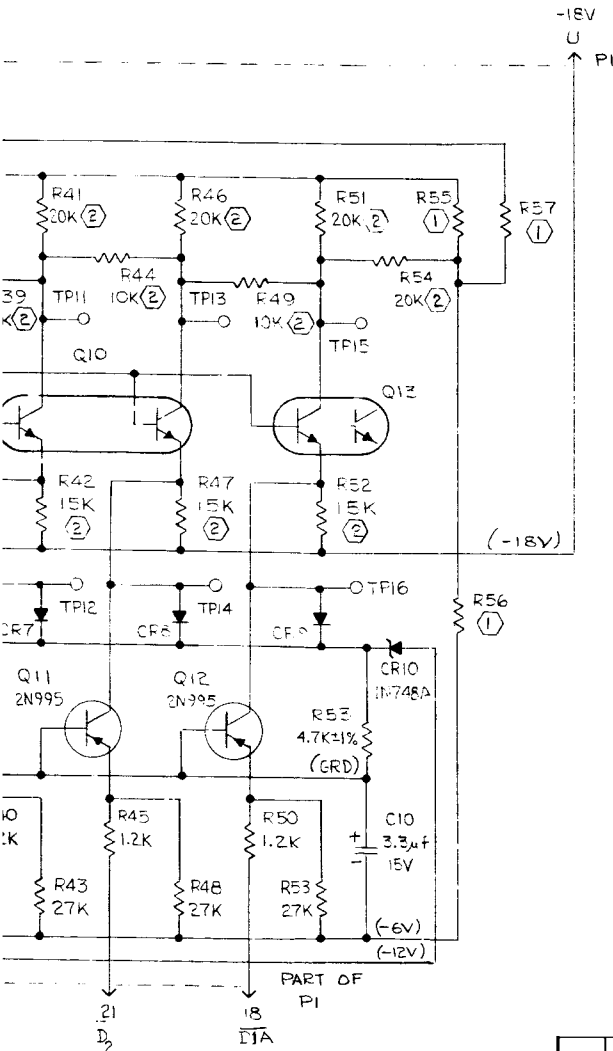
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29	1	MS35233-13	SCREW			
28	1	MS35333-70	WASHER-LK			
27	1	AN960C4L	WASHER-FLAT			
26	1		WIRE	*30	ENAMEL COATED	COML
25	1	100-1	RETAINER TOROID			COML
24	5	K-131	MOUNT-TRANSISTOR			
23	2	SN517	SOLID STATE MODULE WITH MYLAR INSULATOR			COML
22	1	SN515				
21	1	SN514				
20	1	SN512				
19	1	SN511				
18	7	SN510	SOLID STATE MODULE WITH MYLAR INSULATOR			COML
17	5		TRANSISTOR MOUNT	TO-18		COML
16	5	2N2604	TRANSISTOR	TO-18		COML
15	3	1005	TRANSISTOR	TO-5		COML
13	10	1N4153	DIODE			COML
12	1	CYFM5C471G	CAPACITOR	470pf ±2% 500V		COML
11	1	CYFM10C101G	CAPACITOR	100pf ±2% 500V		COML
10	1	KG22J15KMS	CAPACITOR	22μf ±10% 15V		COML
9	10	CO7	RESISTOR	100K ±2% 1/4 W		COML
7	3	CO7	RESISTOR	4.7K ±2% 1/4 W		COML
6	1	CO7	RESISTOR	1K ±2% 1/4 W		COML
4	1	10003-403	TRANSFORMER			
3	16	910443-203	TERMINAL			DSCD
2	1	11412-203-11	TEE-PCB ASSY			
1	1	10351-502-3	PCB	.062 ±.006 × 4.81		
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UNLESS OTHERWISE SPECIFIED						
DIMENSIONS ARE IN INCHES						
TOLERANCES ON						
DECIMALS ANGLES						
XX ±.03 ± 0° 30'						
XXX ±.010						
DRILLED HOLES						
.040 TO .125 ±.002, -.001						
.136 TO .228 ±.003, -.001						
.234 TO .300 ±.004, -.001						
.315 TO .750 ±.005, -.001						
.765 TO 1.000 ±.007, -.001						
1.015 TO 2.000 ±.010, -.001						
DRAWN O. HAMPTON 25 HRS/74						
CHECK						
APPD						
APPD						
FINISH						
HEAT TREAT						
SURFACE ROUGHNESS PER MIL-STD-10						
SCALE: 2 1						
SIZE F						
DO NOT SCALE THIS DRAWING						
WEIGHT						
SHEET						
CALIFORNIA COMPUTER PRODUCTS INC.						
305 MULLER, ANAHEIM, CALIFORNIA						
ANALOG INPUTS & 25KC GENERATOR						
10351-502						

2



9. CAPACITOR  
 8. C11 & C12 LOCAL  
 7. R2 & R15 COM  
 6. REF ASSY  
 5. TRANSISTOR  
 4. DIODE AFF  
 (2) 3. VALUES ±0.0  
 (1) 2. VALUE TO BE  
 1. RESISTOR V  
 NOTE: UNLESS

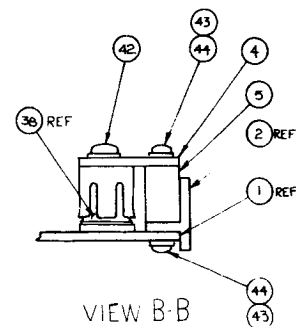
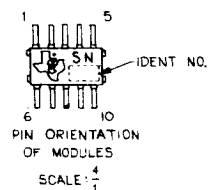
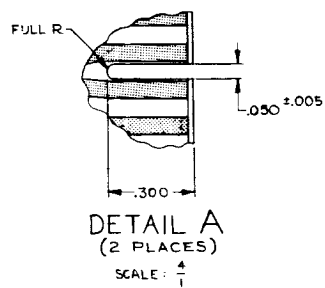
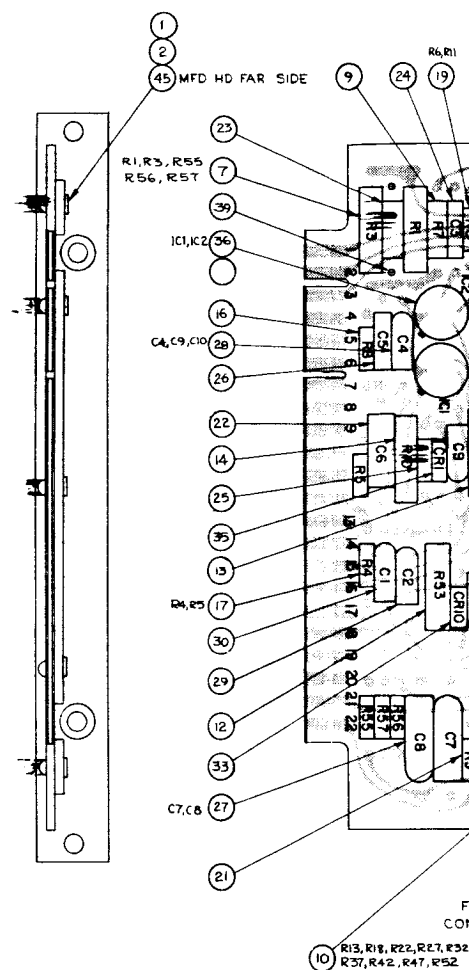
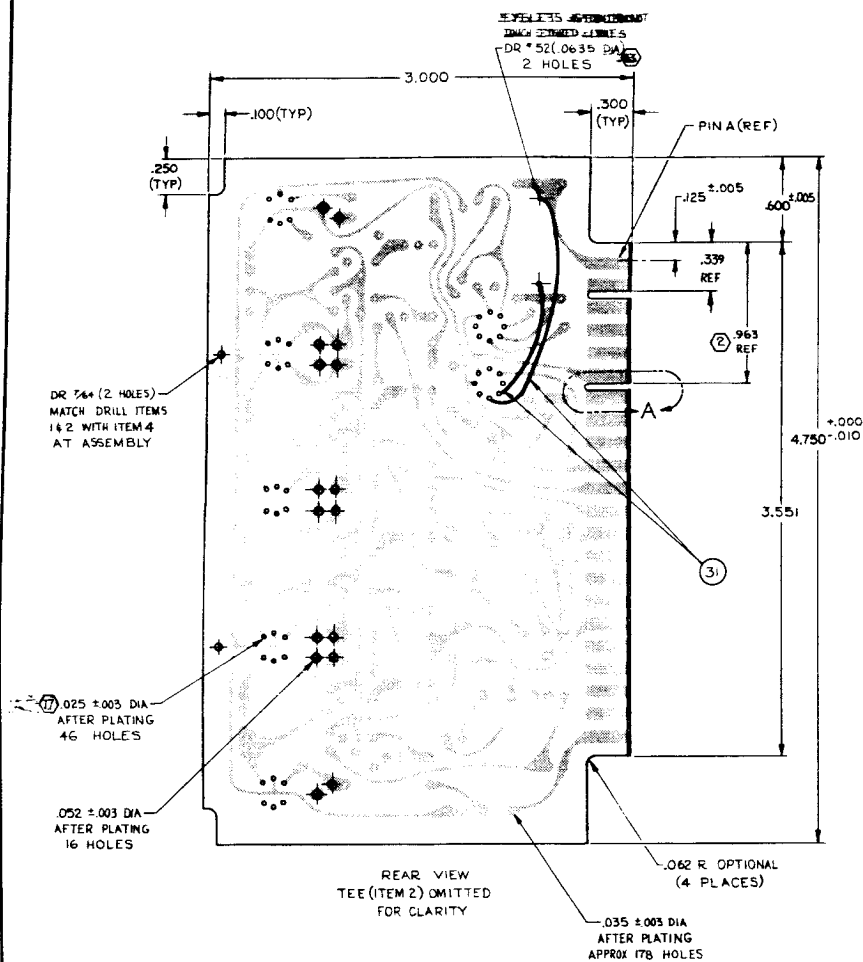
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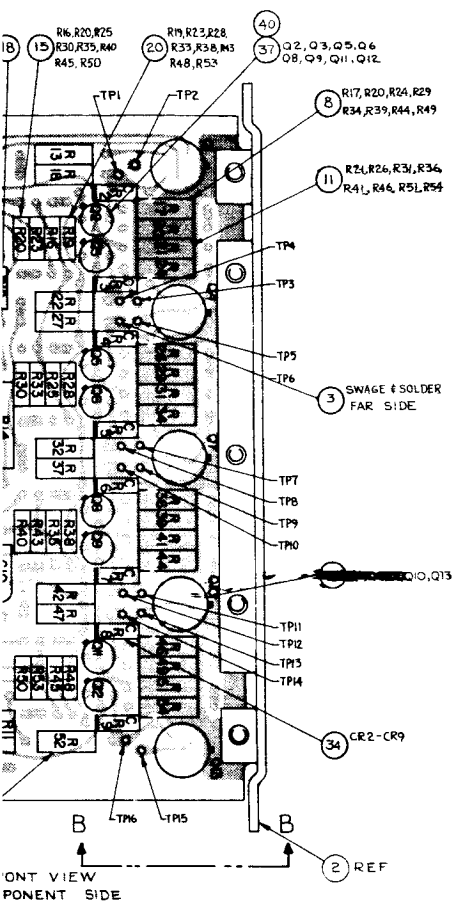
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 IN4153  
 $1\% 0.1W$   
 DETERMINED AT FUNCTIONAL TEST  
 LUET ARE IN CHIMS  $\pm 2\%$  AND ARE  $1/4W$   
 THERWISE SPECIFIED

1	10368-502	SCHEMATIC			
REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION		ZONE
LIST OF MATERIAL OR PARTS LIST					
UNLESS OTHERWISE SPECIFIED		DRAWN	O. HAMPTON	DATE	1964
DIMENSIONS ARE IN INCHES		CHECK			
TOLERANCES ON		APPD			
DECIMALS	ANGLES	APPD			
XX $\pm .03$	$\pm 0^{\circ} 30'$	FINISH			
XXX $\pm .010$		HEAT TREAT			
DRILLED HOLES		SURFACE ROUGHNESS PER MIL-STD-10	✓		
.040	TO .1285: $+.002, -.001$				
.136	TO .228: $+.003, -.001$				
.234	TO .500: $+.004, -.001$				
.515	TO .750: $+.005, -.001$				
.765	TO 1.000: $+.007, -.001$				
1.015	TO 2.000: $+.010, -.001$				
CALIFORNIA COMPUTER PRODUCTS INC. 305 MULLER, ANAHEIM, CALIFORNIA					
SCHEMATIC-					
ANALOG/DIGITAL CONVERTER					
SCALE: NONE		SIZE: D	10368-502		
DO NOT SCALE THIS DRAWING		WEIGHT	SHEET		

2

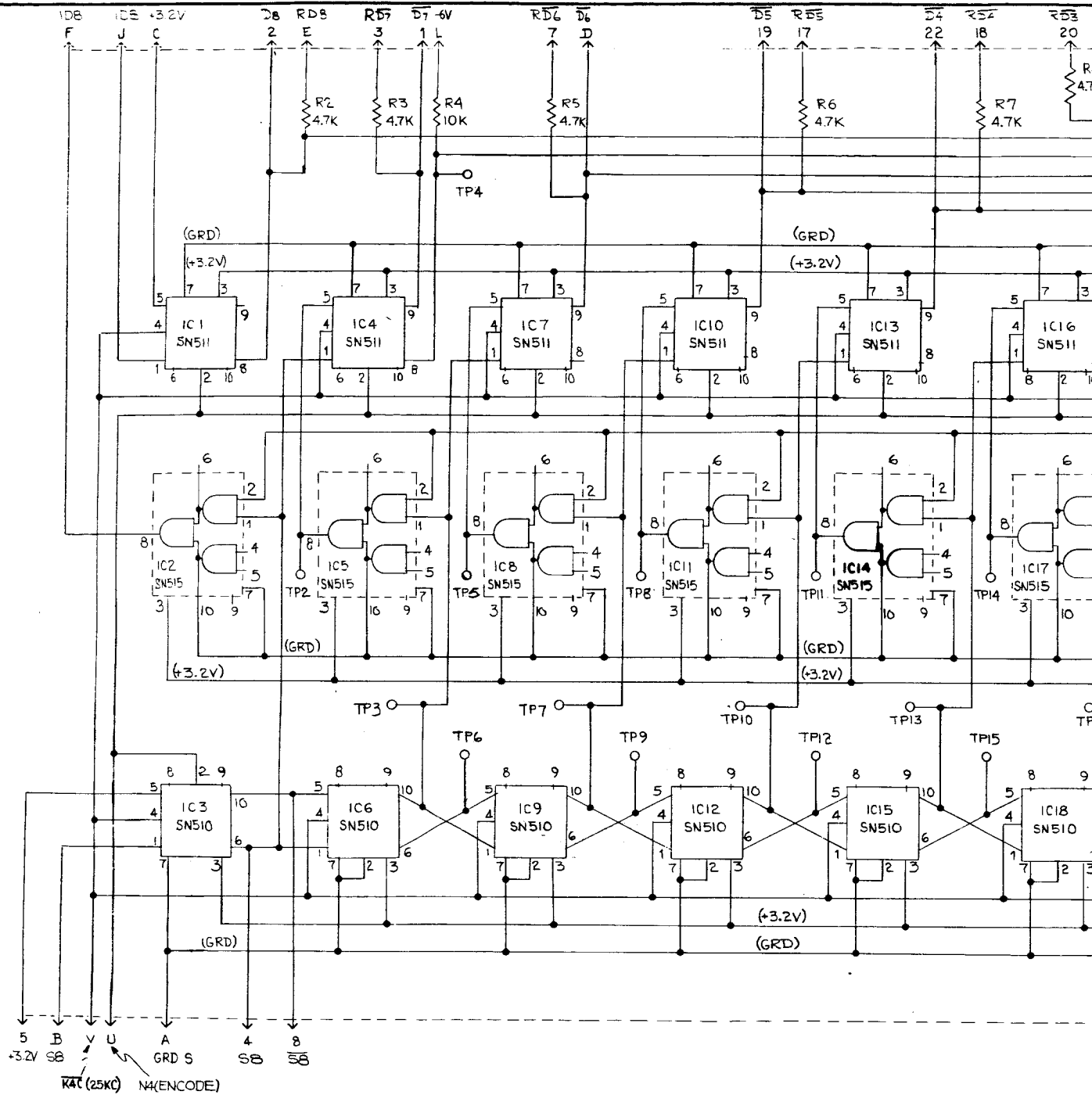


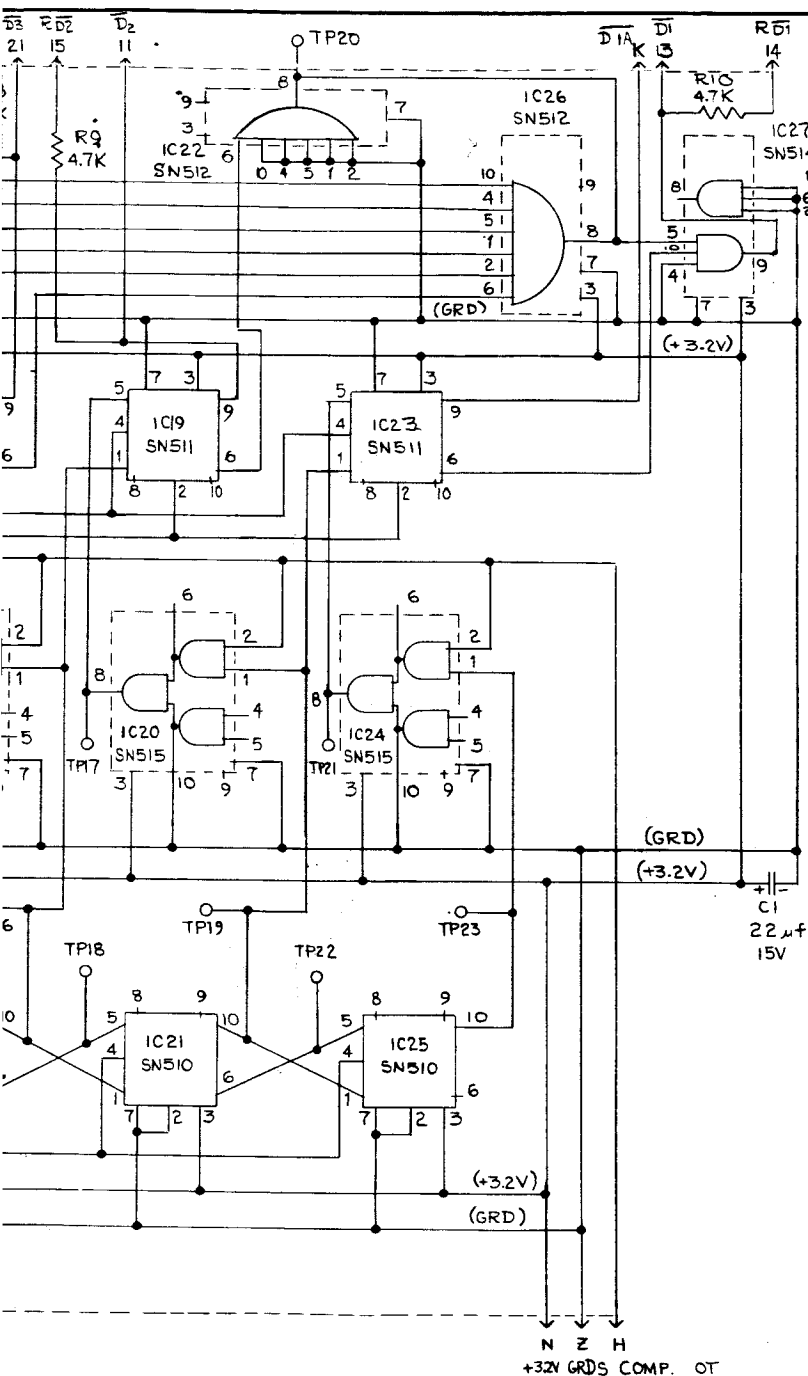




- 27 KIDWELL INC VAN NUYS, CALIF  
 26 TO BE LANDLESS HOLES PER CCP SPEC A0105-007  
 25 REA MAGNETIC WIRE CO INC; FORT WAYNE, IND  
 24 UNITED SHOE MACHINERY CORP, BOSTON, MASS.  
 23 ALLEN BRADLEY CO, MILWAUKEE, WISCONSIN  
 22 DO NOT PLATE THRU  
 21 NATIONAL BERYLLIA CORP; HASKELL, N.J.  
 20 FAIRCHILD SEMICOND DIV; MOUNTAIN VIEW, CALIF  
 19 MOTOROLA SEMICOND PROD; PHOENIX, ARIZ  
 18 GENERAL ELECTRIC SEMICOND DIV, SYRACUSE, N.Y.  
 17 KEMET DEPT UNION CARBIDE CORP CLEVELAND, OHIO  
 16 GENERAL ELECTRIC CO, SCHENECTADY, N.Y.  
 15 CORNING GLASS WORKS, BRADFORD, PA.  
 14 I.R.C.; PHILADELPHIA, PA.  
 13 KELVIN VAN NUYS, CALIF  
 12 VALUE TO BE DETERMINED AT FUNCTIONAL TEST  
 11 REF SCHEMATIC DWG NO. 10368-502  
 10 COMPONENT REF DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND DO NOT APPEAR ON ACTUAL PART.  
 9 KEYSLOT DIMENSIONS ARE FOR REFERENCE ONLY, SLOT SHOULD BE CENTERED BETWEEN PINS AND MUST NOT TOUCH CIRCUITRY.  
 8 MATCH DRILL AND RIVET ITEMS 1 AND 2 USING JIG FIXTURE 11430-203  
 7 FABRICATE PER CCP SPEC A0105-007  
 6 SILK SCREEN USING SSM 10367-502-3  
 5 FABRICATE USING PCM 10367-502-3  
 4 EPOXY GLASS LAMINATE WITH 2 OZ COPPER BOTH SIDES, MIL-P-13949C, TYPE GE  
 3 PLATING:  
 a - COPPER PLATE HOLES .001 MIN  
 b - NICKEL PLATE HOLES AND CIRCUITRY .00050 MIN.  
 c - GOLD PLATE HOLES AND CIRCUITRY .00050 MIN.  
 2 CHAMFER CONNECTOR TIP .020 X .30" BOTH SIDES.  
 1 BOARD THICKNESS AT CONNECTOR TIP NOT TO EXCEED .065 ± .005  
 NOTE: UNLESS OTHERWISE SPECIFIED

45	5	MS20470A2-4	RIVE T				
44	4	MS35233-3	SCREW				
43	4	MS35333-69	WASHER-LOCK				
42	5	30022	RETAINER-TRANSISTOR	TO-5			COML
40	8	JK-131	MOUNT-TRANSISTOR	TO-18			COML
39	2	SE-22	EYELET				
38	5	2N2453	TRANSISTOR				COML
37	8	2N995	TRANSISTOR				
36	2	4A709	OPR. AMPLIFIER				
35	1	1N4574	DIODE				
34	8	1N4153	DIODE				
33	1	1N748A	DIODE				COML
31	1		WIRE	30	ENAMEL COATED		COML
30	1	KG6RBJ6KMS	CAPACITOR	6.8pf ±10% 6V			COML
29	1	KG2R2J20KM5		2.2uf ±10% 20V			
28	3	KG3R3J15KMS		3.3uf ±10% 15V			
27	2	KG6R8J35KMS		6.8uf ±10% 35V			
26	1	CYFM15C68IG		680pf ±2% 300V			
25	1	CYFM10C15IG		150pf ±2% 500V			
24	1	CYFM10C68OG		68pf ±2% 500V			
23	1	CYFM10C10OG		10pf ±2% 500V			
22	1	64F10BC102	CAPACITOR	.001 ±5% 200V			
21	1	CB47G5	RESISTOR	4.7K ±5% 1/4W			
20	8	C07		27K ±2% 1/4W			
19	2			10K			
18	1			4.7K			
17	2			3.3K			
16	1			1.5K			
15	8	C07		1.2K ±2% 1/4W			
14	1	MEA-TO		6K ±1% 1/8W			
13	1	MEA-TO		5.62K ±1% 1/8W			
12	1	MEA-TO		4.7K ±1% 1/8W			
11	8	1318P		20K ±0.5% 1W			
10	9			15K			
9	1			12K			
8	8	1318P		10K ±0.5% 1W			
7	5		RESISTOR	③			COML
5	2	11519-203	SPACER				
4	1	11438-203	HEAT SINK-TRANSISTOR				
3	16	910443-203	TERMINAL				DSCD
2	1	11412-203-51	TEE-PCB ASSY				
1	1	10367-502-3	PCB	.062 × .306 × 4.81		①	
ITEM	1	10367-502	A/D CONV				
NO.	REQD.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION			
LIST OF MATERIAL OR PARTS LIST							
UNLESS OTHERWISE SPECIFIED				DRAWN BY G. HAMPTON TO MEAL			
DIMENSIONS ARE IN INCHES				CALIFORNIA COMPUTER PRODUCTS INC.			
TOLERANCES ON				305 MULLER, ANAHEIM, CALIFORNIA			
DECIMALS				ANGLES			
XX ± .03				± 0° 30'			
XXX ± .010							
DRILLED HOLES				ANALOG/DIGITAL CONVERTER			
.040 TO .125 ± .002 - .001							
.136 TO .228 ± .003 - .001							
.234 TO .500 ± .004 - .001							
.515 TO .750 ± .005 - .001							
.765 TO 1.000 ± .007 - .001							
1.015 TO 2.000 ± .010 - .001							
HEAT TREAT				SCALE: 2			
SURFACE ROUGHNESS PER MIL-STD-10				SIZE F			
				10367-502			
				WEIGHT			
				SHEET			





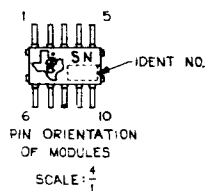
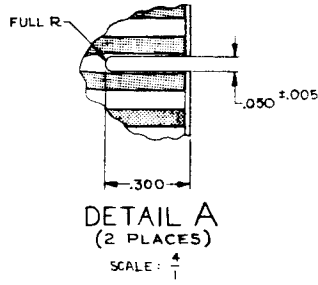
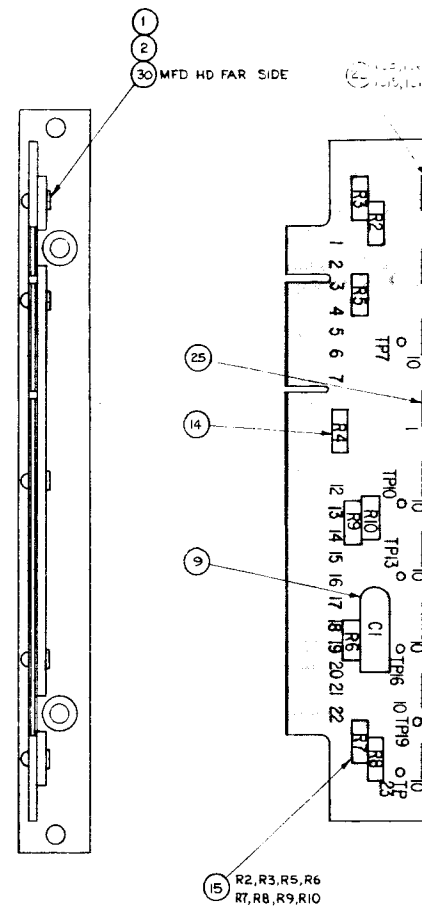
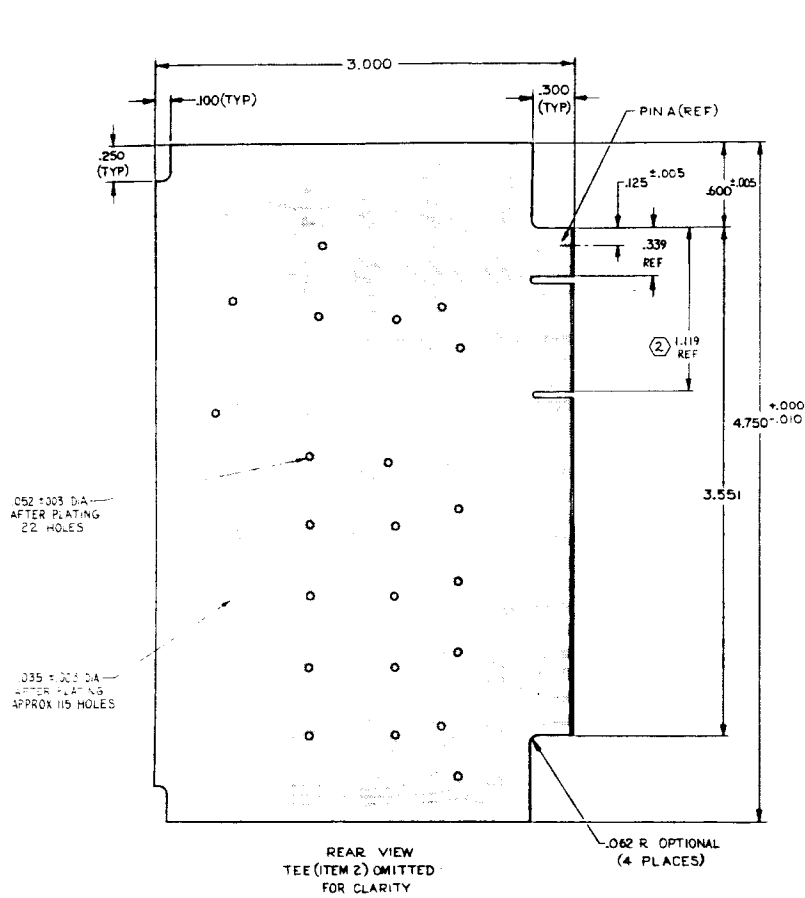
REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
1		MAY BE REWORKED	
2		CANNOT BE REWORKED	
3		NONE	

N Z H  
+32V GRDS COMP. OT

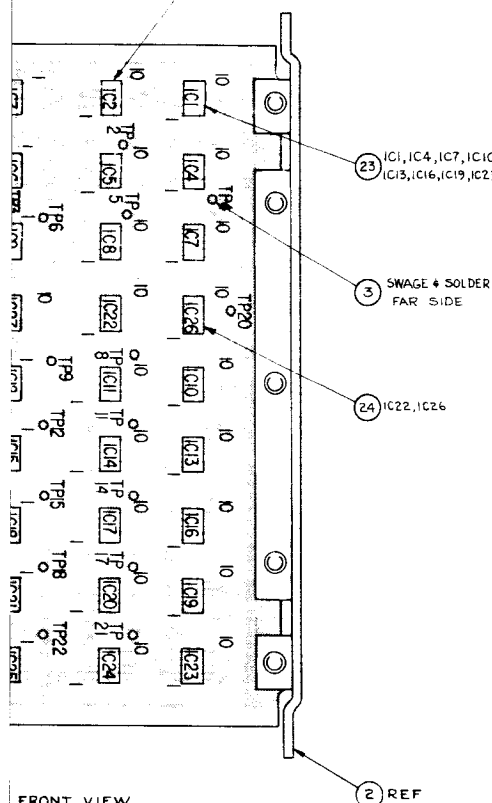
PIERS ARE NOT USED  
EF ASSY DWG NO. 10365-502  
RESISTOR VALUES ARE IN OHMS+2% AND ARE 1/4W  
UNLESS OTHERWISE SPECIFIED

1	10366-502	SCHEMATIC		
REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION	ZONE
LIST OF MATERIAL OR PARTS LIST				
UNLESS OTHERWISE SPECIFIED		DRAWN <i>O. HAMPTON</i>	DATE <i>1/15/66</i>	<b>CALIFORNIA COMPUTER PRODUCTS INC.</b> 305 MULLER, ANAHEIM, CALIFORNIA <b>SCHEMATIC-ANALOG TO DIGITAL DATA CONTROL</b>
DIMENSIONS ARE IN INCHES		CHECK <i>[initials]</i>	<i>5-3-66</i>	
TOLERANCES ON		APPD		
DECIMALS .XX ± .03		APPD		
ANGLES ± 0° 30'		FINISH		
XXX ± .010		HEAT TREAT		
DRILLED HOLES		SURFACE ROUGHNESS PER MIL-STD-10	✓	
.040 TO .1285: +.002, -.001		SCALE: NONE	SIZE: D	10366-502
.136 TO .228: +.003, -.001		DO NOT SCALE THIS DRAWING	WEIGHT	SHEET
.234 TO .500: +.004, -.001				
.515 TO .750: +.005, -.001				
.765 TO 1.000: +.007, -.001				
1.015 TO 2.000: +.010, -.001				

2



1. IC2, IC5, IC8, IC11  
IC14, IC7, IC20, IC24

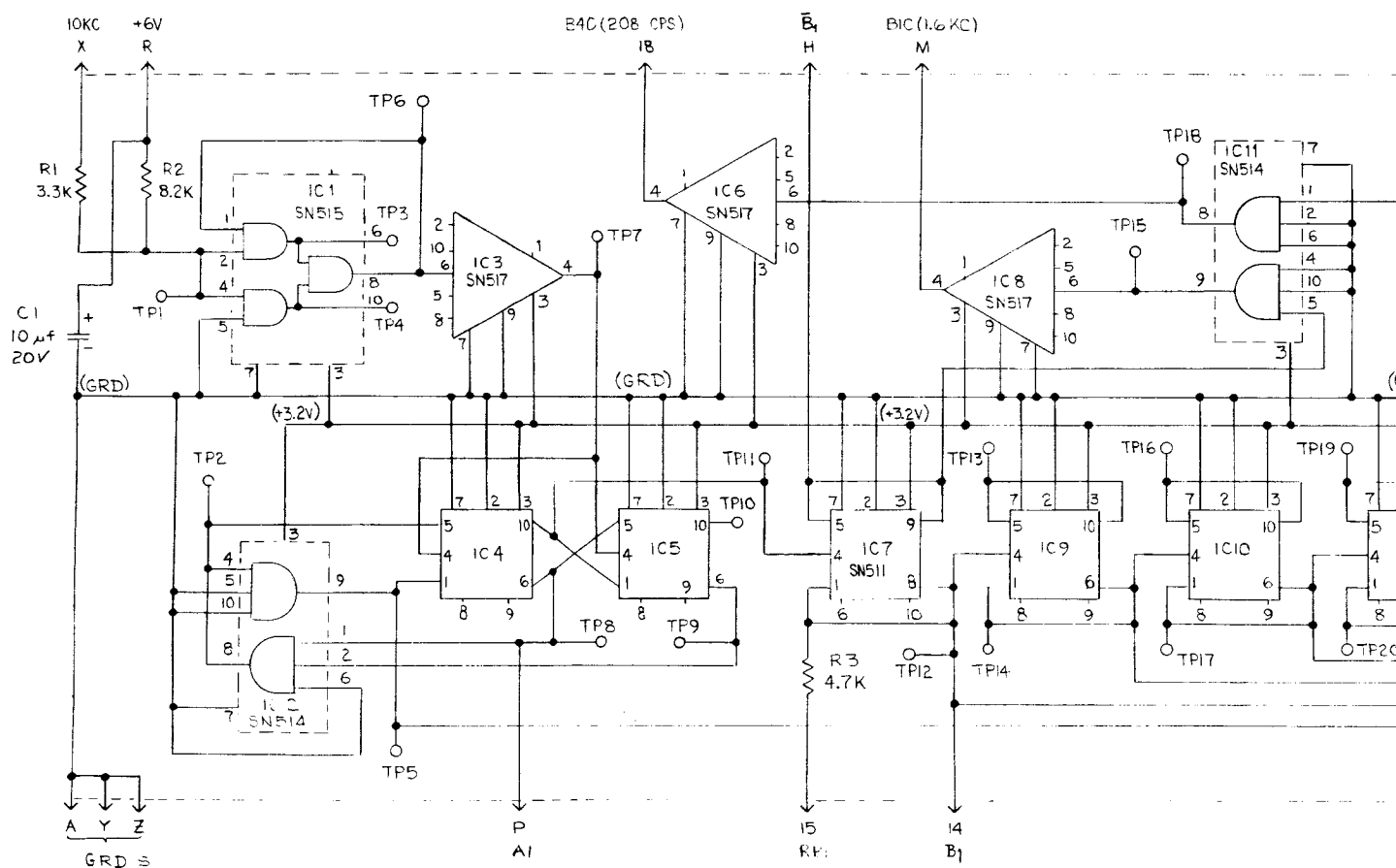


FRONT VIEW  
COMPONENT SIDE

5. TEXAS INSTRUMENTS INC, DALLAS, TEXAS
  4. CORNING GLASS WORKS, PHILADELPHIA, PA
  3. KEMET DEPT UNION CARBIDE CORP, CLEVELAND, OHIO
  1. REF SCHEMATIC DWG NO. 10366-502
  10. COMPONENT REF DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND DO NOT APPEAR ON ACTUAL PART.
  2. KEYSLOT DIMENSIONS ARE FOR REFERENCE ONLY, SLOT SHOULD BE CENTERED BETWEEN PINS AND MUST NOT TOUCH CIRCUITRY.
  8. MATCH DRILL AND RIVET ITEMS 1 AND 2 USING JIG FIXTURE 11430-203
  7. FABRICATE PER CCP SPEC A0105-007
  6. SILK SCREEN USING SSM 10365-502-3 REV A
  5. FABRICATE USING PCM 10365-502-3 REV A
  4. EPOXY GLASS LAMINATE WITH 2 OZ COPPER BOTH SIDES, MIL-P-13949C, TYPE GE
  3. PLATING:
    - a - COPPER PLATE HOLES .001 MIN
    - b - NICKEL PLATE HOLES AND CIRCUITRY .00050 MIN.
    - c - GOLD PLATE HOLES AND CIRCUITRY .000050 MIN.
  2. CHAMFER CONNECTOR TIP .020 X 30° BOTH SIDES.
  1. BOARD THICKNESS AT CONNECTOR TIP NOT TO EXCEED .065 ± .008
- NOTE: UNLESS OTHERWISE SPECIFIED

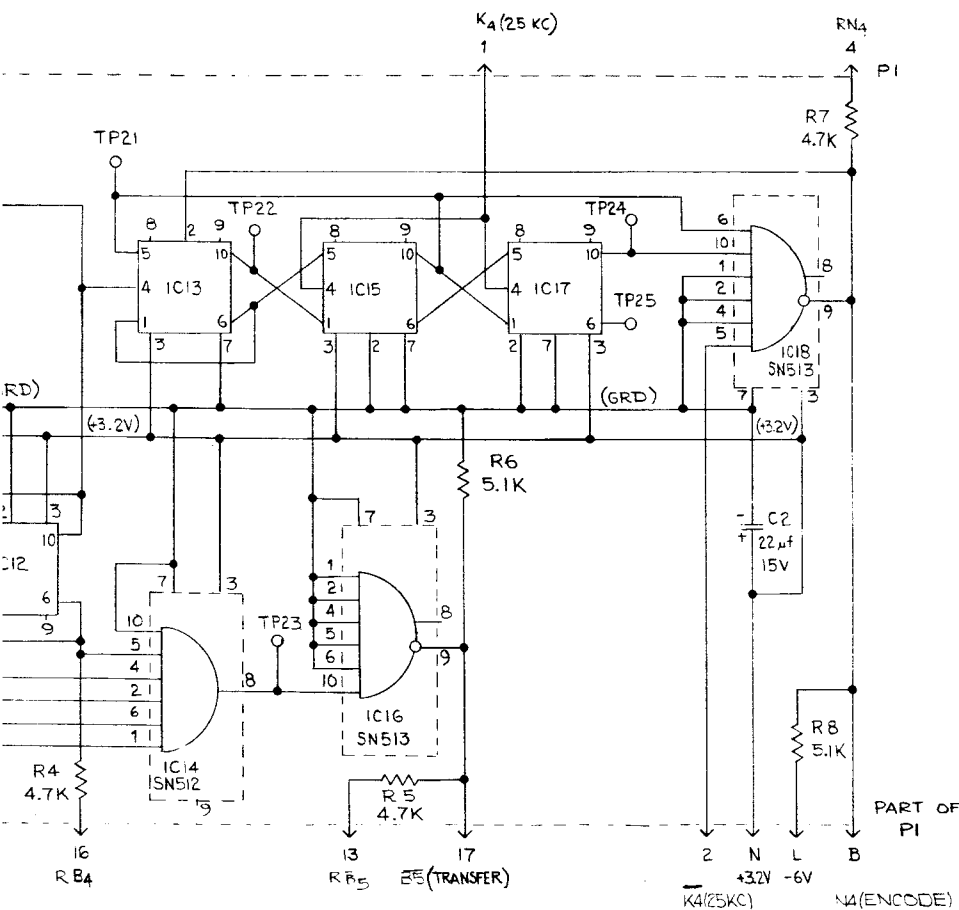
SYN		77	REVISIONS		DATE & APPROVAL
			DESCRIPTION		
			MAY BE REWORKED	1	
			CANNOT BE REWORKED	2	
			NONE	3	

30	5	MS20470A2-4	RIVET						
26	8	SN515	SOLID STATE MODULE WITH MYLAR INSULATOR					COML	
25	1	SN514							
24	2	SN512							
23	8	SN511							
22	8	SN510	SOLID STATE MODULE WITH MYLAR INSULATOR					COML	
15	8	CO7	RESISTOR	47K ± 2% 1/4 W				COML	
14	1	CO7	RESISTOR	10K ± 2% 1/4 W				COML	
9	1	KG22J15KM5	CAPACITOR	22uf ± 10% 15V				COML	
3	22	910443-203	TERMINAL					DISC	
2	1	11412-203-41	TEE-PCB ASSY						
1	1	10365-502-3	PCB	.062 ± .006 X 4.8					
ITEM NO.	1	10365-502	A/D DATA CONTROL						
NO.	RECD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		MATERIAL				ZONE
					SIZE, DESCRIPTION & SPECIFICATION				
LIST OF MATERIAL OR PARTS LIST									
UNLESS OTHERWISE SPECIFIED			DRAWN C. HAMPTON		CALIFORNIA COMPUTER PRODUCTS INC.				
DIMENSIONS ARE IN INCHES			CHECK		305 MULLER, ANAHEIM, CALIFORNIA				
TOLERANCES ON			APPRO		ANALOG/DIGITAL DATA CONTROL				
DECIMALS			APPRO						
XX ± .03			FINISH						
XXX ± .010			HEAT TREAT						
DRILLED HOLES					SCALE: 1/1		SIZE: F		10365-502
.040 TO .1285 ± .002 - .001					DO NOT SCALE THIS DRAWING		WEIGHT		
.136 TO .228 ± .003 - .001							SHEET		
.234 TO .300 ± .004 - .001									
.315 TO .750 ± .005 - .001									
.765 TO 1.000 ± .007 - .001									
1.015 TO 2.000 ± .010 - .001			SURFACE ROUGHNESS PER MIL-STD-10 ✓						



3. REVER  
2. RESIS  
1. ALL IN  
NOTE UN

REVISIONS				DATE & APPROVAL	
SYM	ZONE	DESCRIPTION		DATE	APPROVAL
1		MAY BE REWORKED			
2		CANNOT BE REWORKED			
3		NONE			



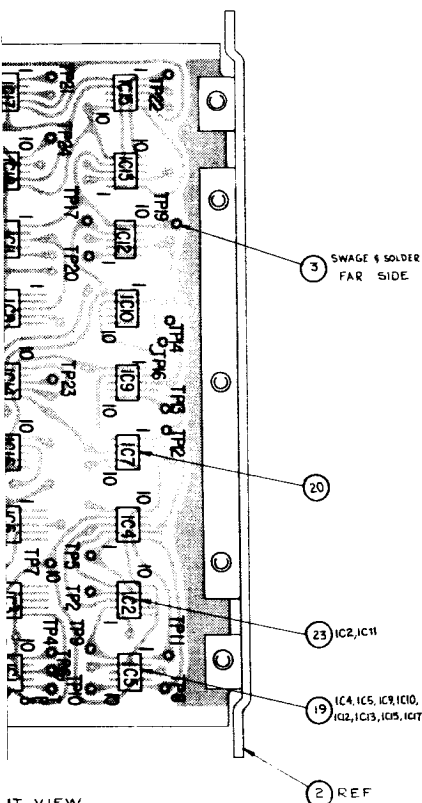
NOT ASSY L.V.G NO.10352-502  
 VALUES ARE IN OHMS  $\pm 2\%$  AND ARE  $\frac{1}{4}W$   
 INTEGRATED CIRCUITS ARE SN510  
 UNLESS OTHERWISE SPECIFIED

10352-502		SCHEMATIC			
REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		MATERIAL SIZE, DESCRIPTION & SPECIFICATION	
LIST OF MATERIAL OR PARTS LIST					
UNLESS OTHERWISE SPECIFIED		DRAWN O. HANAPTON 12-9-65		CALIFORNIA COMPUTER PRODUCTS INC.	
DIMENSIONS ARE IN INCHES		CHECK 5-3-66		305 MULLER, ANAHEIM, CALIFORNIA	
TOLERANCES ON		APPD		SCHEMATIC - ENCODE-TIMING GENERATOR	
DECIMALS		APPD			
XX $\pm .03$		FINISH		SCALE: NONE	
XXX $\pm .010$		HEAT TREAT		SIZE D	
DRILLED HOLES		SURFACE ROUGHNESS PER MIL-STD-10		10352-502	
.040 TO .1285: $+.002, -.001$		✓		DO NOT SCALE THIS DRAWING	
.136 TO .228: $+.003, -.001$				WEIGHT	
.234 TO .500: $+.004, -.001$				SHEET	
.515 TO .750: $+.005, -.001$					
.765 TO 1.000: $+.007, -.001$					
1.015 TO 2.000: $+.010, -.001$					

2







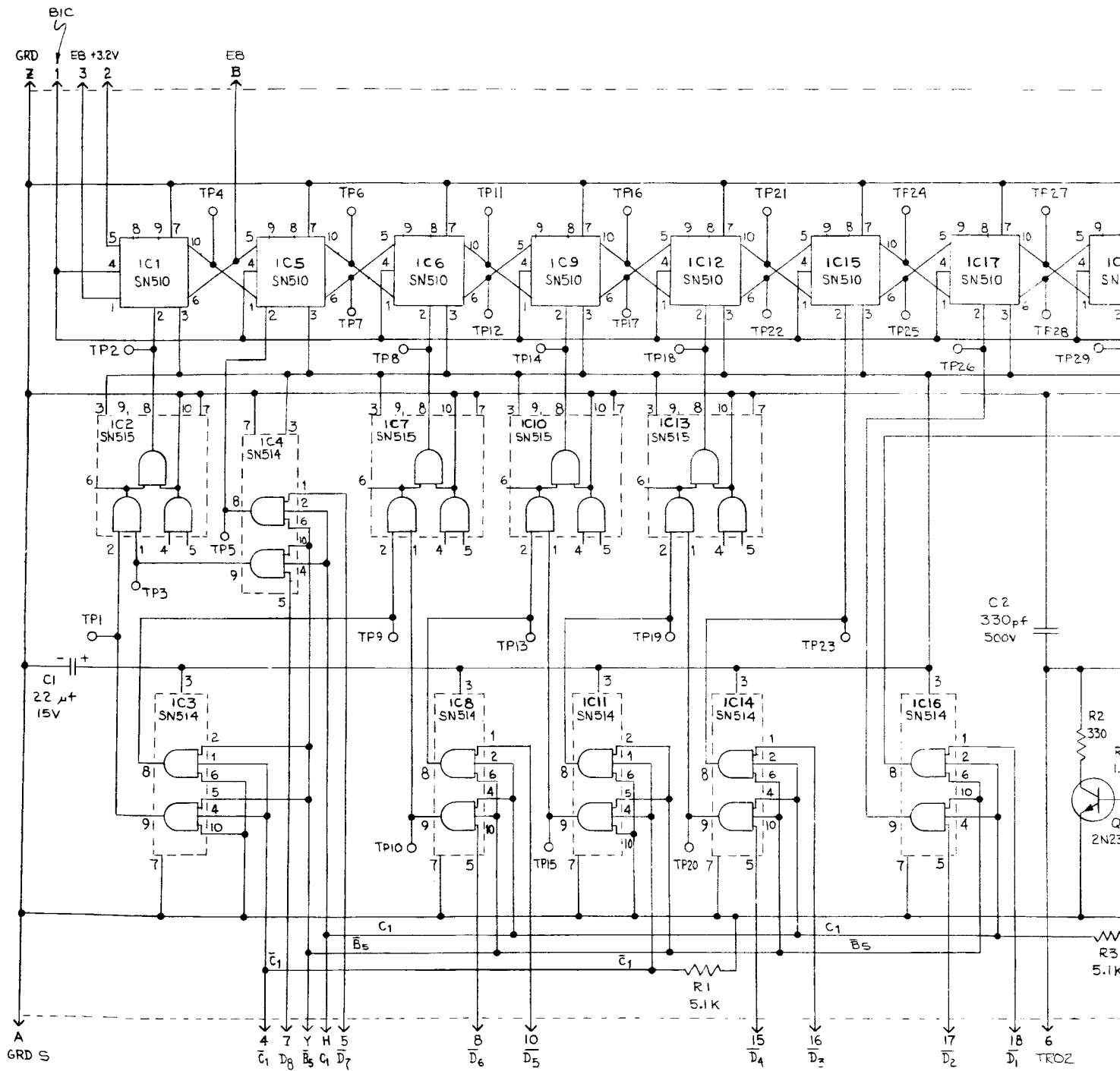
IT VIEW  
NENT SIDE

5. H. TEXAS INSTRUMENTS INC, DALLAS, TEXAS.
6. KEMET DEPT UNION CARBIDE INC, CLEVELAND, OHIO
7. CORNING GLASS WORKS, BRADFORD, PA
8. REF SCHEMATIC DWG NO. 10352-502
9. COMPONENT REF DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND DO NOT APPEAR ON ACTUAL PART.
10. KEYSLOT DIMENSIONS ARE FOR REFERENCE ONLY, SLOT SHOULD BE CENTERED BETWEEN PINS AND MUST NOT TOUCH CIRCUITRY.
11. MATCH DRILL AND RIVET ITEMS 1 AND 2 USING JIG FIXTURE 11430-203
12. FABRICATE PER CCP SPEC AD105-007
13. SILK SCREEN USING SSM 10353-502-3
14. FABRICATE USING PCM 10353-502-3
15. EPOXY GLASS LAMINATE WITH 2 OZ COPPER BOTH SIDES, MIL-P-13949C, TYPE GE
16. PLATING:
  - a - COPPER PLATE HOLES .001 MIN
  - b - NICKEL PLATE HOLES AND CIRCUITRY .00050 MIN.
  - c - GOLD PLATE HOLES AND CIRCUITRY .000050 MIN.
17. CHAMFER CONNECTOR TIP .020 X 30° BOTH SIDES.
18. BOARD THICKNESS AT CONNECTOR TIP NOT TO EXCEED .065 ± .005
- NOTE: UNLESS OTHERWISE SPECIFIED

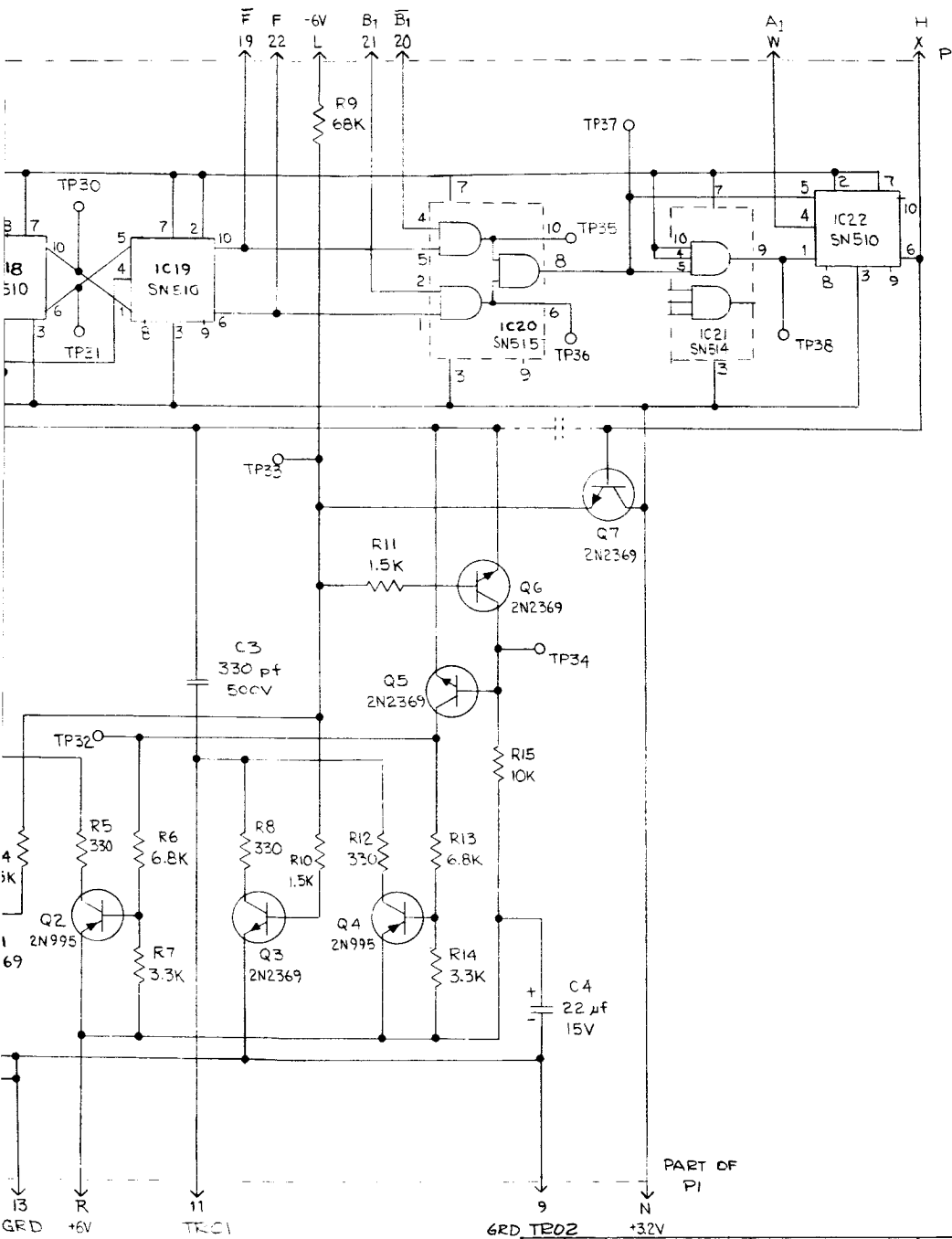
SYN		ZONE		REVISIONS		DATE & APPROVAL	
SYN		ZONE		DESCRIPTION		DATE & APPROVAL	
				1 MAY BE REWORKED		2 CANNOT BE REWORKED	
				3 NONE			

30	5	MS20470A2-4	RIVET						
25	3	SN517	SOLID STATE MODULE WITH MYLAR INSULATOR					COML	
24	1	SN515							
23	2	SN514							
22	2	SN513							
21	1	SN512							
20	1	SN511							
19	8	SN510	SOLID STATE MODULE WITH MYLAR INSULATOR					COML	
15	1	KG22J15KMS	CAPACITOR	22 $\mu$ f $\pm$ 10% 15V				COML	
14	1	KG10J20KMS	CAPACITOR	10 $\mu$ f $\pm$ 10% 20V				COML	
10	1	CO7	RESISTOR	8.2K $\pm$ 2% 1/4W				COML	
9	2			5.1K					
8	4			4.7K					
7	1	CO7	RESISTOR	3.3K $\pm$ 2% 1/4W				COML	
3	25	9,0443-203	TERMINAL					DSCD	
2	1	11412-203-21	TEE-PCB ASSY						
1	1	10353-502-3	PCB	.062 $\pm$ 3.06 $\times$ 4.81					
ITEM NO.	REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION				ZONE	
LIST OF MATERIAL OR PARTS LIST									
UNLESS OTHERWISE SPECIFIED			DRAWN	O. HAMPTON 25 MCH/64					
DIMENSIONS ARE IN INCHES			CHECK						
TOLERANCES ON			APPD						
DECIMALS			APPD						
ANGLES			FINISH						
X.X $\pm$ .03									
X.XX $\pm$ .010									
DRILLED HOLES									
.040 TO .1285 $\pm$ .002 - .001									
.136 TO .228 $\pm$ .003 - .001									
.234 TO .500 $\pm$ .004 - .001									
.515 TO .750 $\pm$ .005 - .001									
.765 TO 1.000 $\pm$ .007 - .001									
1.015 TO 2.000 $\pm$ .010 - .001									
HEAT TREAT									
SURFACE ROUGHNESS PER MIL-STD-10									
SCALE: $\frac{2}{1}$				SIZE: F		10353-502			
DO NOT SCALE THIS DRAWING				WEIGHT		SHEET			

2



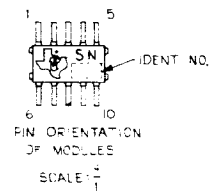
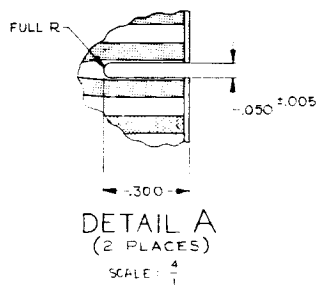
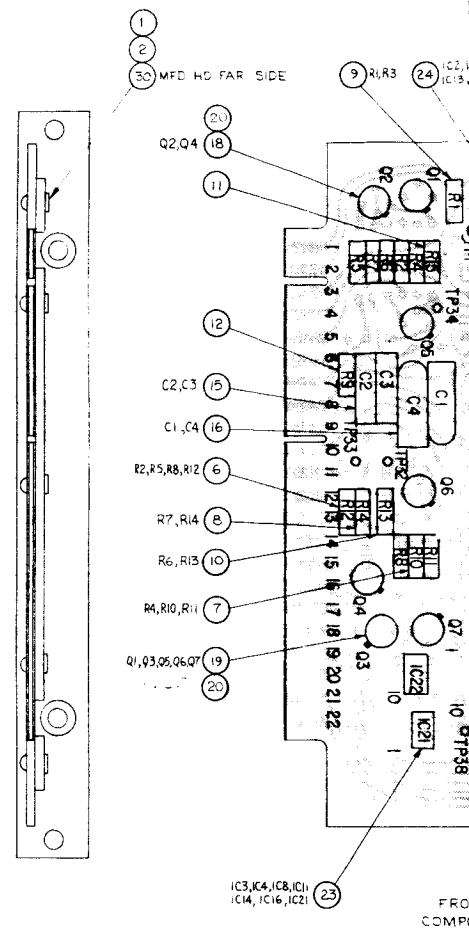
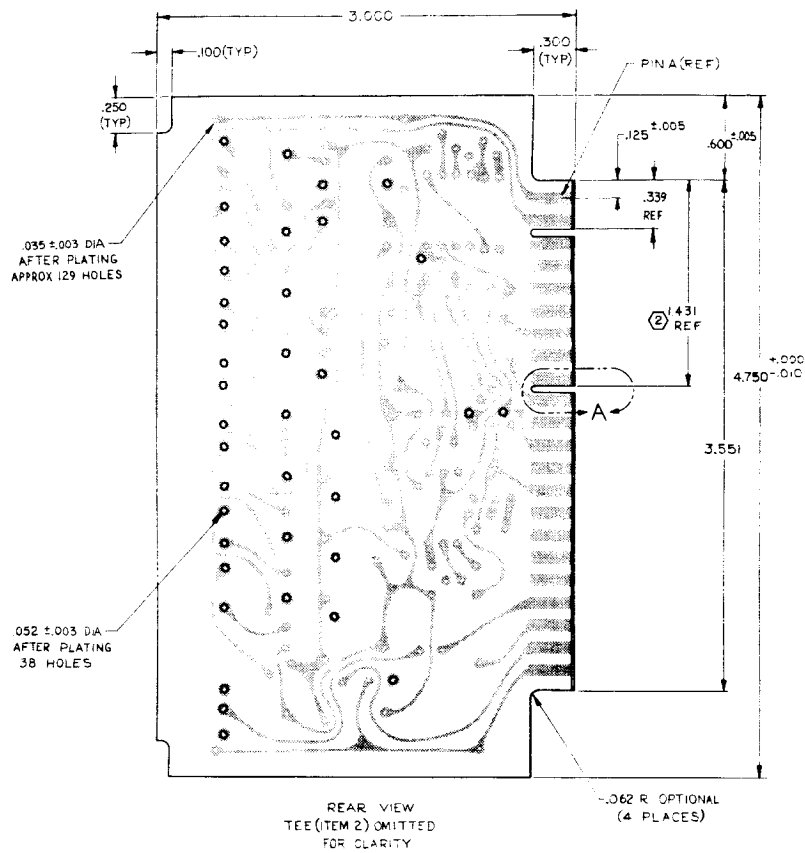
REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
1		MAY BE REWORKED	
2		CANNOT BE REWORKED	
3		NONE	



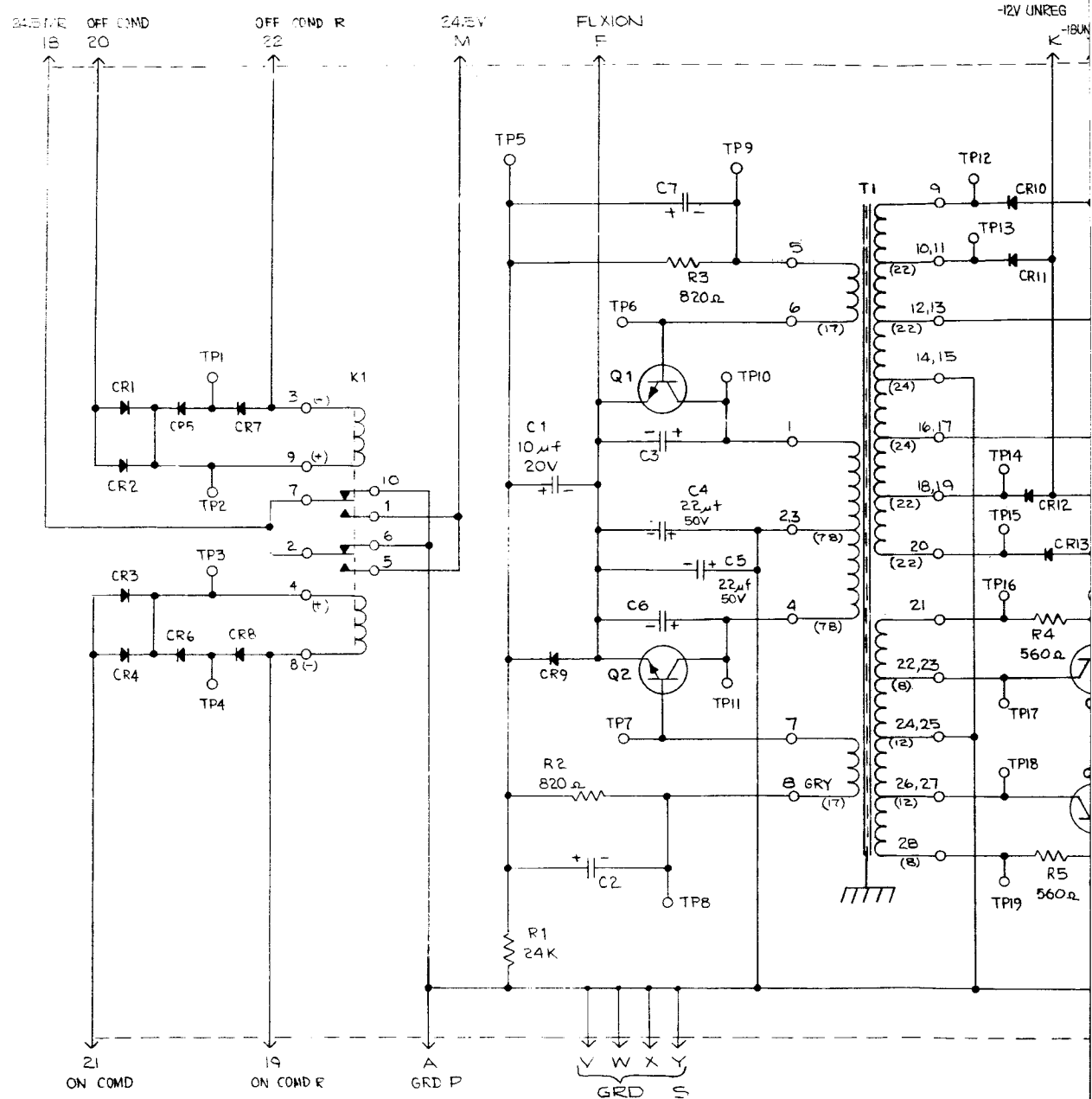
REQD		PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION		MATERIAL SIZE, DESCRIPTION & SPECIFICATION		ZONE	
LIST OF MATERIAL OR PARTS LIST									
UNLESS OTHERWISE SPECIFIED		DRAWN		O. Hampton		20 Dec 65		CALIFORNIA COMPUTER PRODUCTS INC. 305 MULLER, ANAHEIM, CALIFORNIA	
DIMENSIONS ARE IN INCHES TOLERANCES ON  DECIMALS   ANGLES .XX ± .03   ± 0° 30' .XXX ± .010		CHECK		5-3-66					
		APPD							
		APPD							
		FINISH							
DRILLED HOLES  .040 TO .1285: +.002, -.001 .136 TO .228: +.003, -.001 .234 TO .500: +.004, -.001 .515 TO .750: +.005, -.001 .765 TO 1.000: +.007, -.001 1.015 TO 2.000: +.010, -.001		HEAT TREAT		SCALE: NONE		SIZE D		10354 - 502	
		SURFACE ROUGHNESS PER MIL-STD-10		DO NOT SCALE THIS DRAWING		WEIGHT			
								SHEET	

EF ASSY DWG NO. 10354-502  
RESISTOR VALUES ARE IN OHMS ± 2% AND ARE 1/4W  
E UNLESS OTHERWISE SPECIFIED

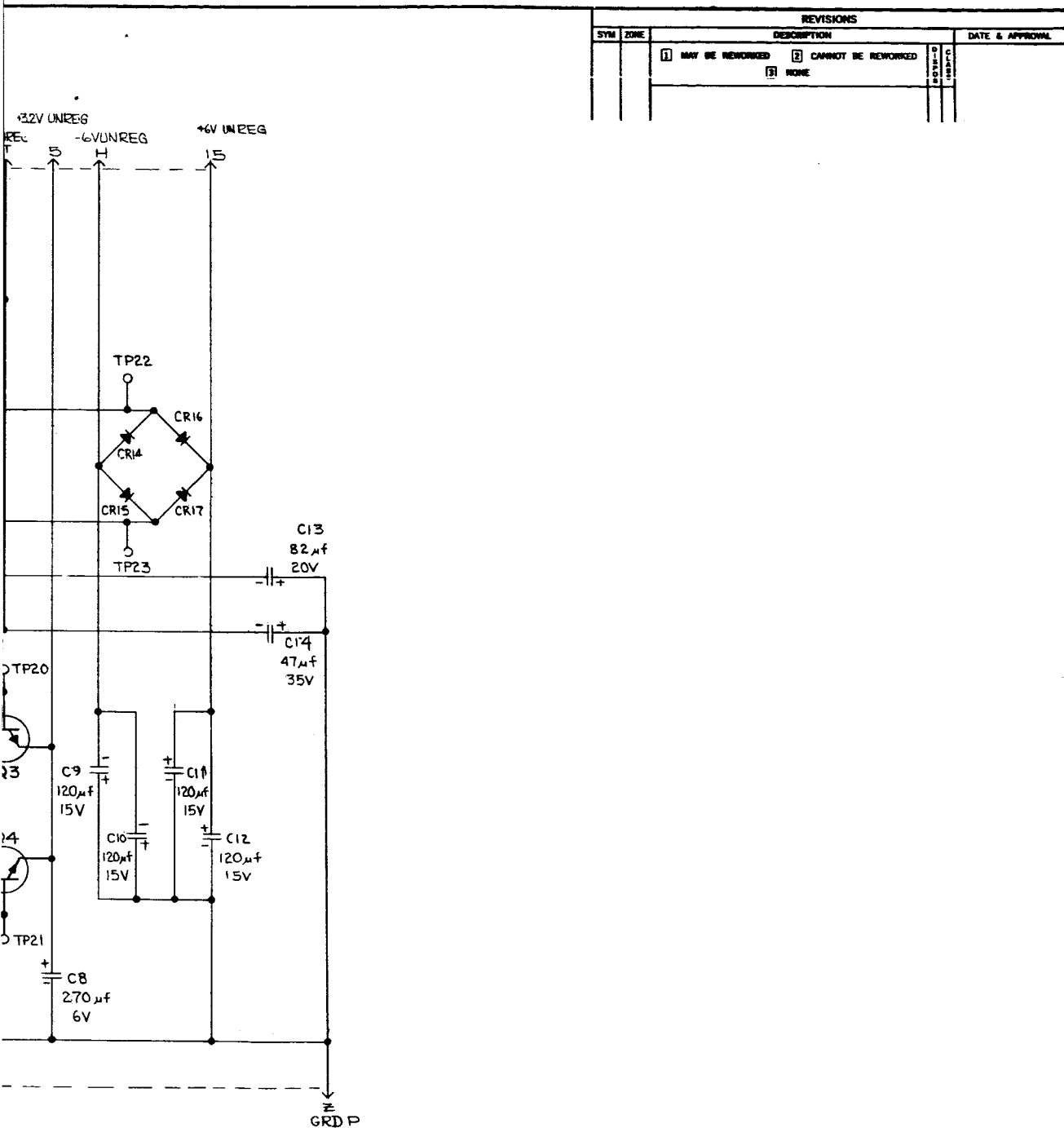
2







5 RESISTOR VALUES ARE IN OHMS  
 4. REF ASSY DWG NO. 10370-5  
 3. CAPACITOR VALUES ARE IN MIC  
 2. TRANSISTORS ARE 2N2658  
 1. DIODES ARE 1N3730  
 NOTE UNLESS OTHERWISE SPECIF



2% AND ARE 1/4W  
02  
0.05 FARADS ± 10%

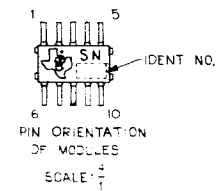
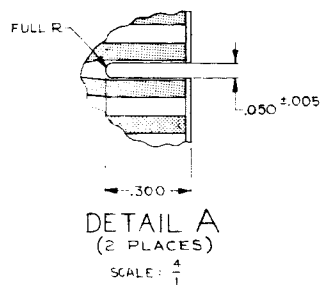
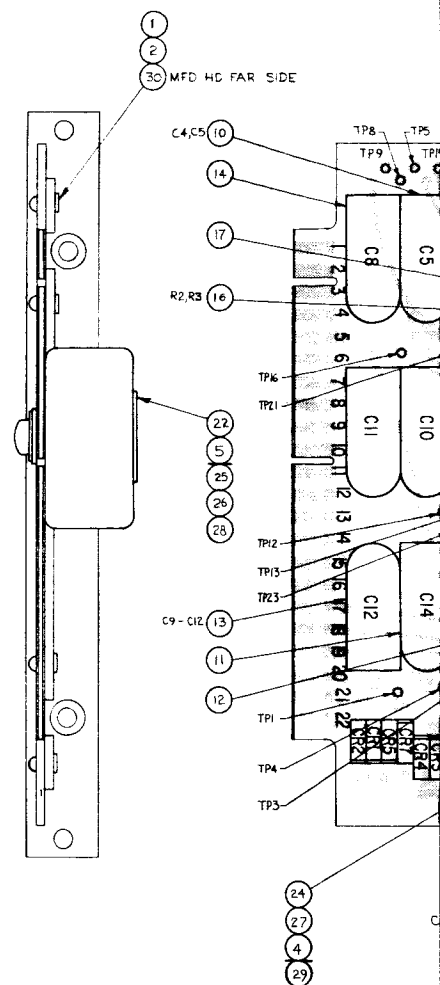
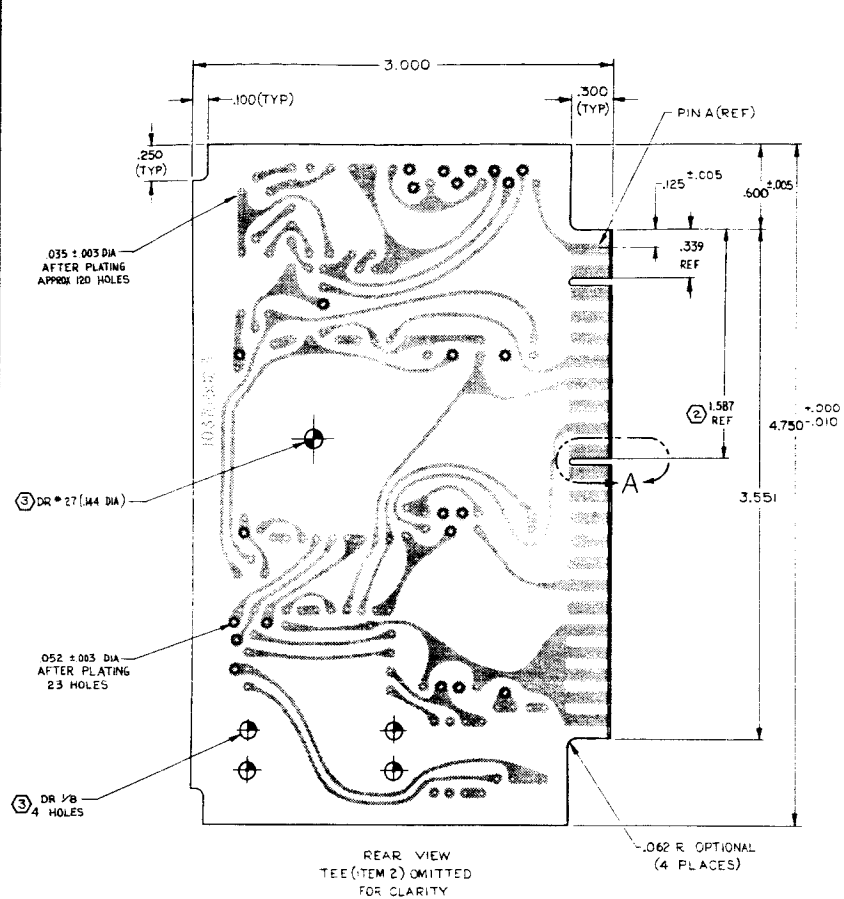
ED

1	10369-502	SCHEMATIC			
REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SIZE, DESCRIPTION & SPECIFICATION	MATERIAL	ZONE
LIST OF MATERIAL OR PARTS LIST					
UNLESS OTHERWISE SPECIFIED		DRAWN	O. H. HAMPTON 18 JAN, 1964		
DIMENSIONS ARE IN INCHES		CHECK	5-3-64		
TOLERANCES ON		APPD			
DECIMALS		APPD			
ANGLES		FINISH			
XX ± .03					
XXX ± .010		HEAT TREAT			
DRILLED HOLES		SURFACE ROUGHNESS PER MIL-STD-10	✓		
.040 TO .1285: +.002, -.001					
.136 TO .228: +.003, -.001					
.234 TO .500: +.004, -.001					
.515 TO .750: +.005, -.001					
.765 TO 1.000: +.007, -.001					
1.015 TO 2.000: +.010, -.001					
SCALE: NONE			SIZE: D	10369-502	
DO NOT SCALE THIS DRAWING			WEIGHT	SHEET	

CALIFORNIA COMPUTER PRODUCTS INC.  
305 MULLER, ANAHEIM, CALIFORNIA

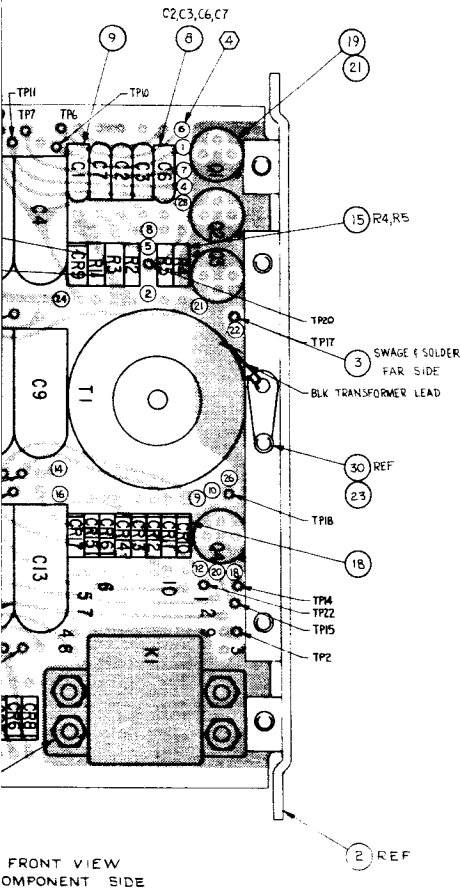
SCHEMATIC-  
DC TO DC CONVERTER  
NO. 1

12





REVISIONS				
SYM	ZONE	DESCRIPTION		DATE & APPROVAL
		1 MAY BE REWORKED	2 CANNOT BE REWORKED	DATE TIME BY CHECKED
		3 NONE		

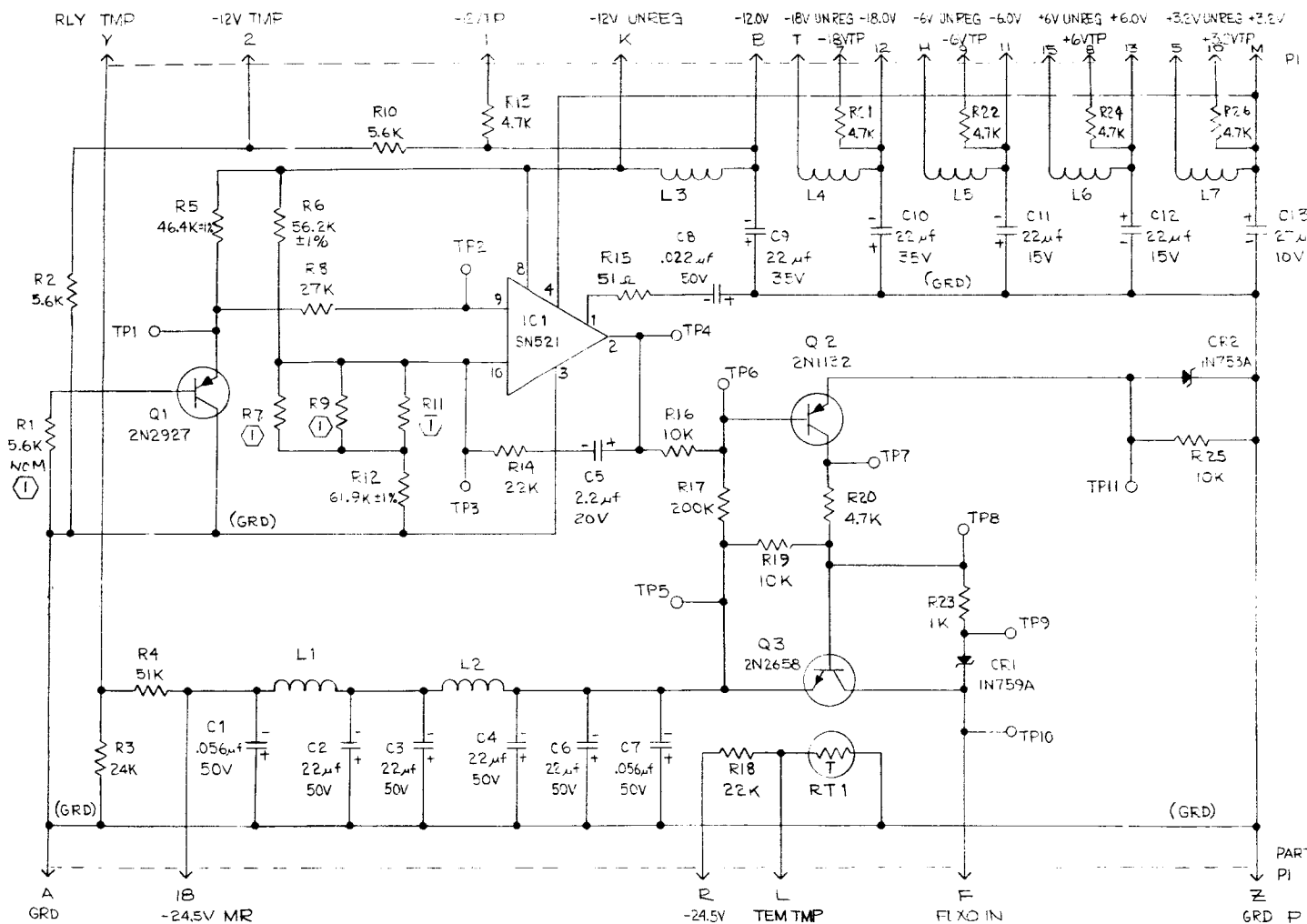


FRONT VIEW  
COMPONENT SIDE

- ① 20 HERMAN H SMITH CO, BROOKLYN, NY  
 ② 9 MODULAR ELECTRONICS, INGLEWOOD, CALIF  
 ③ 18 DELBERT BLINN CO INC, POMONA, CALIF  
 ④ 17 HONEYWELL SEMI COND DIV, RIVERA BEACH, FLA  
 ⑤ 16 RAYTHEON CO SEMI COND DIV, NEEDHAM HEIGHTS, MASS  
 ⑥ 15 CORNING GLASS WORKS, BRADFORD, PA  
 ⑦ 14 KEMET DEPT UNION CARBIDE CORP CLEVELAND, OHIO  
 ⑧ 13 TRANSFORMER LEADS TO BE SOLDERED AT PLACES INDICATED  
 ⑨ 12 DO NOT PLATE THRU  
 ⑩ REF SCHEMATIC DWG NO. 103369-502  
 ⑪ COMPONENT REF DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND DO NOT APPEAR ON ACTUAL PART.  
 ⑫ KEYHOLE DIMENSIONS ARE FOR REFERENCE ONLY. SLOT SHOULD BE CENTERED BETWEEN PINS AND MUST NOT EXCEED .001 INCH.  
 ⑬ MATCH DRILL AND RIVET ITEMS 1 AND 2 USING JIG PART # 1450-203  
 ⑭ FABRICATE PER COR SPEC ADIOS-007  
 ⑮ BLK SCREEN USING SEM 10370-502-3  
 ⑯ FABRICATE USING FORM 10370-502-3  
 ⑰ EPOXY GLASS LAMINATE WITH 2.0Z COTTER BOTH SIDES. MIL-P-13349D, TYPE 3E  
 ⑱ PLATING:  
 a - COPPER PLATE HOLES .0001 MIN.  
 b - NICKEL PLATE HOLES AND CROUTRY .00050 MIN.  
 c - GOLD PLATE HOLES AND CROUTRY .00050 MIN.  
 ⑲ CHAMFER CONNECTOR TIP .030 X .30" BOTH SIDES.  
 ⑳ BOARD THICKNESS AT CONNECTOR TIP NOT TO EXCEED .065-.068  
 NOTE: UNLESS OTHERWISE SPECIFIED

NO.	REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SIZE, DESCRIPTION & SPECIFICATION	MATERIAL	ZONE
30	5	MS20470A2-4	RIVET			
29	4	MS35233-13	SCREW			
28	1	MS35233-31	SCREW			
27	4	MS35333-70	WASHER-LOCK			
26	1	MS35333-71	WASHER-LOCK			
25	1	AN960C6L	WASHER-FLAT			
24	4	AN340C4	NUT- HEX			
23	1	1485-6	LUG			COML
22	1	100-4	RETAINER-TOROID			COML
21	4	FP-50	MOUNT-TRANSISTOR	TO-5		COML
19	4	2N2658	TRANSISTOR	TO-5		COML
18	17	1N3730	DIODE			
17	1	C07	RESISTOR	24K ±2% 1/4W		
16	2	C07	RESISTOR	820K ±2% 1/4W		
15	2	C07	RESISTOR	560K ±2% 1/4W		
14	1	KG2TOJ6KMS	CAPACITOR	270μf ±10% 6V		
13	4	KG120J15KMS		120μf ±10% 15V		
12	1	KG82J20KMS		82μf ±10% 20V		
11	1	KG47J35KMS		47μf ±10% 35V		
10	2	KG22J50KMS		22μf ±10% 50V		
9	1	KG10J20KMS		10μf ±10% 20V		
8	4	KG022J50KMS	CAPACITOR	0.022μf ±10% 50V		COML
5	1	91005-403	TRANSFORMER			DISC
4	1	11508-203	RELAY			
3	23	90443-203	TERMINAL			DISC
2	1	11412-203-61	TEE-PCB ASSEMBLY			
1	1	10370-502-3	PCB	2.0Z COTTER		
1	1	10370-502	DC/DC CONV #1			
LIST OF MATERIAL OR PARTS LIST						
UNLESS OTHERWISE SPECIFIED			DRAWN BY: HAMPTON			
DIMENSIONS ARE IN INCHES			CHECK			
TOLERANCES ON			APPD			
DECIMALS			APPD			
XX ± .03			FINISH			
XXX ± .010						
ANGLES						
± 0° 30'						
DRILLED HOLES						
.040	TO .125	± .002 - .001				
.136	TO .228	± .003 - .001				
.234	TO .500	± .004 - .001				
.515	TO .750	± .005 - .001				
.765	TO 1.000	± .007 - .001				
1.015	TO 2.000	± .010 - .001				
HEAT TREAT						
SURFACE ROUGHNESS PER MIL-STD-10						
			✓			
SCALE:			SIZE:		WEIGHT:	
			F			
DO NOT SCALE THIS DRAWING			SHEET			
			10370-502			

2



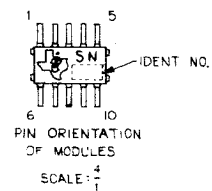
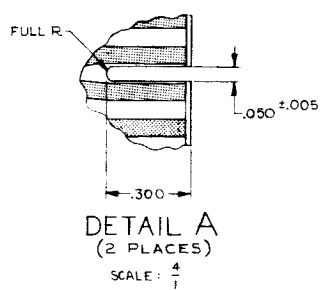
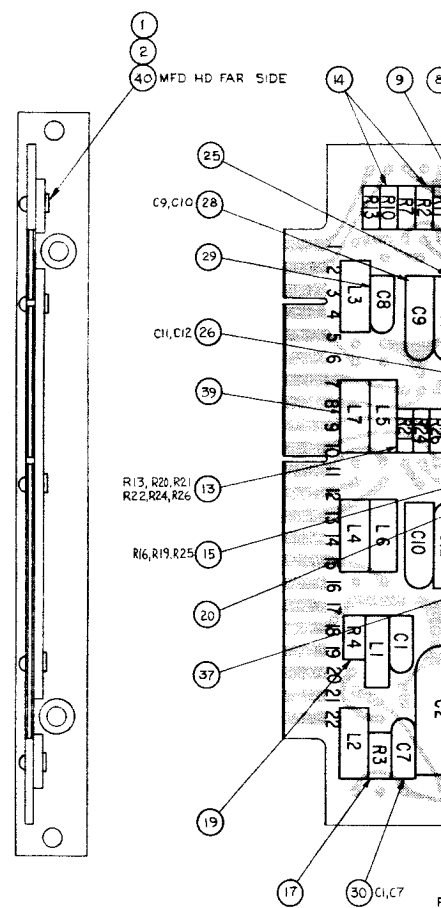
5. CAPACITOR  
4. REF. ASSY  
① 3. VALUE TO  
2. CHOKES AP  
1. RESISTOR  
NOTE: UNLESS

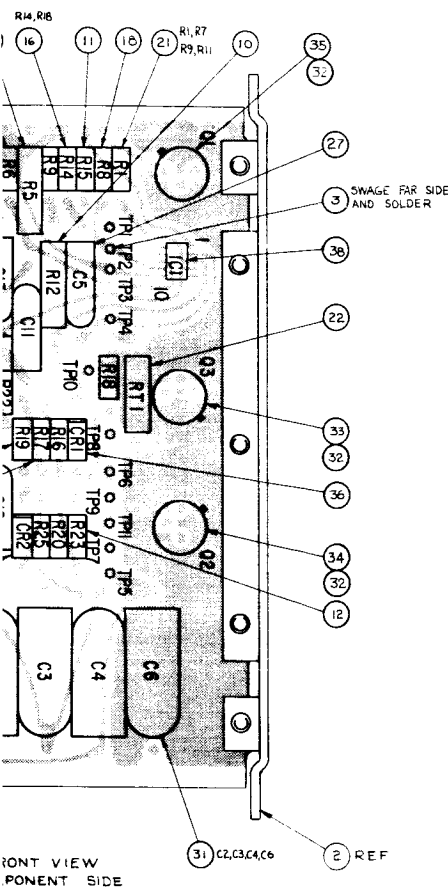
REVISIONS			
SYM	ZONE	DESCRIPTION	DATE & APPROVAL
		1 MAY BE REWORKED	2 CANNOT BE REWORKED
		3 NONE	

1	10372-502	SCHEMATIC				
REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION			ZONE
LIST OF MATERIAL OR PARTS LIST						
UNLESS OTHERWISE SPECIFIED		DRAWN	CHECK	CALIFORNIA COMPUTER PRODUCTS INC. 305 MULLER, ANAHEIM, CALIFORNIA		
DIMENSIONS ARE IN INCHES TOLERANCES ON		APPD	APPD	SCHEMATIC - DC TO DC CONVERTER NO. 2		
DECIMALS	ANGLES	FINISH		SCALE:	SIZE	
.XX ± .03	± 0° 30'	HEAT TREAT		NONE	D	10372-502
XXX ± .010		SURFACE ROUGHNESS PER MIL-STD-10		DO NOT SCALE THIS DRAWING	WEIGHT	SHEET
DRILLED HOLES						
.040 TO .128:	+.002, -.001					
.136 TO .228:	+.003, -.001					
.234 TO .500:	+.004, -.001					
.515 TO .750:	+.005, -.001					
.765 TO 1.000:	+.007, -.001					
1.015 TO 2.000:	+.010, -.001					

VALUES ARE IN MICRO FARADS ± 10%  
 Y DAG NO. 10371-502  
 BE DETERMINED AT FUNCTIONAL TEST  
 CE TYPE 9320-30, 10-44  
 VALUES ARE IN OHMS ± 2% AND ARE 1/4W  
 OTHERWISE SPECIFIED

21





- 13 DELBERT BLINN CO INC, POMONA, CALIF  
 21 J.W. MILLER CO, LOS ANGELES, CALIF  
 11 MOTOROLA SEMICOND PROD INC, PHOENIX, ARIZ  
 19 SYLVANIA ELECTRIC PROD INC, WOBURN, MASS  
 9 FAIRCHILD SEMICONDUCTOR DIV, MOUNTAINVIEW, CALIF  
 17 HONEYWELL SEMICONDUCTOR DIV, RIVIERA BEACH, FLA  
 16 KEMET DEPT UNION CARBIDE CORP, CLEVELAND, OHIO  
 15 TEXAS INSTRUMENTS CORP, DALLAS, TEXAS  
 14 CORNING GLASS WORKS, BRADFORD, PA  
 13 INTERNATIONAL RESISTANCE CORP, PHILADELPHIA, PA  
 12 VALUE TO BE DETERMINED AT FUNCTIONAL TEST  
 11 REF SCHEMATIC DWG NO. 10372-502  
 10 COMPONENT REF DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND DO NOT APPEAR ON ACTUAL PART.  
 9 KEYSLOT DIMENSIONS ARE FOR REFERENCE ONLY, SLOT SHOULD BE CENTERED BETWEEN PINS AND MUST NOT TOUCH CIRCUITRY.  
 8 MATCH DRILL AND RIVET ITEMS 1 AND 2 USING JIG FIXTURE 11430-003  
 7 FABRICATE PER CCP SPEC A0105-007  
 6 SILK SCREEN USING SSM 10371-502-3  
 5 FABRICATE USING PCM 10371-502-3  
 4 EPOXY GLASS LAMINATE WITH 2 OZ COPPER BOTH SIDES, M-L-P-33490, TYPE GE  
 3 PLATING:  
 a - COPPER PLATE HOLES .001 MIN  
 b - NICKEL PLATE HOLES AND CIRCUITRY .00050 MIN.  
 c - GOLD PLATE HOLES AND CIRCUITRY .000050 MIN.  
 2 CHAMFER CONNECTOR TIP .020 X 30° BOTH SIDES.  
 1 BOARD THICKNESS AT CONNECTOR TIP NOT TO EXCEED .065 ± .005  
 NOTE: UNLESS OTHERWISE SPECIFIED

REVISIONS							
SYN	ZONE	DESCRIPTION				DATE & APPROVAL	
		1	MAY BE REMOVED			2	CANNOT BE REMOVED
			3			NONE	

40	5	MS20470A2-4	RIVET						
39	7	9320-30	CHOKE	10 $\mu$ h $\pm$ 10%					COML
38	1	SN521	SOLID STATE MODULE	WITH MYLAR INSULATOR					
37	1	IN753A	DIODE ZENER						
36	1	IN759A	DIODE ZENER						
35	1	2N2927	TRANSISTOR						
34	1	2N1132	TRANSISTOR						
33	1	2N2658	TRANSISTOR						COML
32	3	FP-50	MOUNT-TRANSISTOR						COML
31	4	KG22J50KMS	CAPACITOR	22 $\mu$ f $\pm$ 10% 50V					COML
30	2	KG8056J50KMS		056 $\mu$ f $\pm$ 10% 50V					
29	1	KG8022J50KMS		022 $\mu$ f $\pm$ 10% 50V					
28	2	KG22J35KMS		22 $\mu$ f $\pm$ 10% 35V					
27	1	KG2R2J20KMS		2.2 $\mu$ f $\pm$ 10% 20V					
26	2	KG22J15KMS		22 $\mu$ f $\pm$ 10% 15V					
25	1	KG27J10KMS	CAPACITOR	27 $\mu$ f $\pm$ 10% 10V					COML
24									
23									
22	1	TM-1/8	SENSISTOR	2.2K $\pm$ 5% 1/8W					COML
21	4	C07	RESISTOR	3 $\pm$ 2% 1/4W					
20	1			200K					
19	1			51K					
18	1			27K					
17	1			24K					
16	2			22K					
15	3			10K					
14	2			5.6K					
13	6			4.7K					
12	1			1K					
11	1	C07		51 $\Omega$ $\pm$ 2% 1/4W					
10	1	MEA-TO		619K $\pm$ 1% 1/8W					
9	1	MEA-TO		562K $\pm$ 1% 1/8W					
8	1	MEA-TO	RESISTOR	464K $\pm$ 1% 1/8W					COML
7									
6									
5									
4									
3	11	910443-203	TERMINAL						DISCO
2	1	11412-203-71	TEE-PCB ASSY						
1	1	10371-502-3	PCB	.062 $\times$ 3.06 $\times$ 4.81					
ITEM NO.	REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION		ZONE			
LIST OF MATERIAL OR PARTS LIST									
UNLESS OTHERWISE SPECIFIED			DRAWN	CALIFORNIA COMPUTER PRODUCTS INC.					
DIMENSIONS ARE IN INCHES			CHECK	305 MULLER, ANAHEIM, CALIFORNIA					
TOLERANCES ON			APPD	DC/DC CONVERTER NO 2					
DECIMALS			APPD						
XXX $\pm$ .03			FINISH	10371-502					
XXX $\pm$ .010			HEAT TREAT						
DRILLED HOLES			SURFACE ROUGHNESS PER MIL-STD-10	DO NOT SCALE THIS DRAWING					
.040 TO .125 $\pm$ .002 - .001				WEIGHT					
.136 TO .228 $\pm$ .003 - .001				SHEET					
.234 TO .500 $\pm$ .004 - .001									
.515 TO .750 $\pm$ .005 - .001									
.765 TO 1.000 $\pm$ .007 - .001									
1.015 TO 2.000 $\pm$ .010 - .001									

2

APPENDIX B

MRIR TELEMETRY UNIT  
INPUT/OUTPUT  
INTERFACE SPECIFICATION

Input Connector J1

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
1	Spare	
2	-24.5 DRA	Connected to the negative terminal of the satellite primary regulated supply. To be used by the radio-meter drive amplifiers.
3	----	Spare pin
4	OFFCMD	65-ms pulse with a nominal amplitude of +12 volts to the ON-OFF relay. Input impedance is 160 ohms. Relay is turned off.
5	OFFCMDR	Relay OFF command return line
6	----	Spare pin
7	GRD S	MRIR signal ground
8	GRD P	Power ground connected to the positive terminal of the satellite regulated supply.

Input Connector J1 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
9	-24.5 M	Connected to the negative terminal of the satellite primary regulated supply.
10	-24.5 TM	Connected to the negative terminal of the satellite primary regulated supply. To be used by the thermistor. Input impedance is nominal 2K ohms.
11	ONCMD	65-ms pulse with a nominal amplitude of +12 volts to the ON-OFF relay. Input impedance is 160 ohms. Relay is turned on.
12	ONCMDR	Relay ON command return line.
13	----	Spare pin
14	GRD T	Telemetry ground
15	GRD C	Chassis ground



Output Connector J2

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
1	TRO 1	Tape Recorder Output No. 1 amplitude is +6.5 volts to +5.0 volts for the high state and 0 volts $\pm$ 0.6 volts for the low state. Output impedance is 330 ohms.
2	----	Spare pin
3	GRD TRO 1	Tape Recorder Output No. 1 reference ground
4	GRD TRO 2	Tape Recorder Output No. 2 reference ground
5	GRD P	Power ground
6	TRO 2	Tape Recorder Output No. 2 characteristics are same as TRO 1, Pin 1.
7	GRD S	Signal ground
8	GRD T	Telemetry ground
9	GRD C	Chassis ground

Input/Output Connector J3

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
1	-24.5 MR	Negative terminal of the satellite primary regulated supply. Primary power is routed through the MRIR unit to the radiometer.
2	-24.5 RDA	Negative terminal of the satellite primary regulated supply. Primary power is routed through the MRIR unit to the radiometer driver amplifier.
3	----	Spare pin
4	CH 1	Radiometer Analog Input No. 1 voltage amplitude is 0 volts to -6.4 volts at a frequency up to 8 cps. Input impedance is greater than 150K ohms when the analog gate is on.
5	CH 2	Radiometer Analog Input No. 2 (Same description as Pin 4.)
6	CH 3	Radiometer Analog Input No. 3 (Same description as Pin 4.)
7	GRD S	Signal ground

Input/Output Connector J3 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
8	GRD P	Power ground connected to positive terminal of the satellite primary regulated supply.
9	100 ØA	Output Phase A of a 2-phase, 100-cps, square wave signal which is routed through the MRIR unit to the radio-meter. Amplitude is $-1.5 \pm 1.0$ volt for the high level and $-23.0 \pm 1.5$ volts for the low level.
10	100 ØB	Output Phase B of a 2-phase, 100-cps, square signal which is routed through the MRIR unit to the radio-meter. Phase B leads Phase A by $90^\circ$ . Amplitude same as Phase B.
11	----	Spare
12	CH 4	Radiometer Analog Input No. 4 (Same description as Pin 4.)
13	CH 5	Radiometer Analog Input No. 5 (Same description as Pin 4.)
14	GRD T	Telemetry ground
15	GRD C	Chassis ground

Output Connector J4

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
1	RLY TMP	Relay Telemetry Point Output. Voltage amplitude for on condition is $8 \pm 1.5$ volts and $0 \pm 0.6$ volts for the off condition. Output impedance is 16.3K ohms.
2	TEM TMP	Temperature Telemetry Point Output. Voltage amplitude is variable between -1.3 volts and -3.0 volts over the temperature range of $-10^{\circ}\text{C}$ to $+65^{\circ}\text{C}$ . Output impedance is less than 3K ohms over the temperature range. The output voltage is derived from a separate -24.5 volt supply.
3	----	Spare
4	-18V TP	MRIR -18 volts $\pm 3$ percent regulated secondary supply. Provides 4.7K-ohm isolation resistor on output.
5	-12V TP	MRIR -12 volts $\pm 3$ percent regulated secondary supply. Provides 4.7K-ohm isolation resistor on output.

Output Connector J4 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
6	-6V TP	MRIR -6 volts $\pm 3$ percent regulated secondary supply. Provides a 4.7K-ohm isolation resistor on output.
7	+6V	MRIR +6 volts $\pm 3$ percent regulated secondary supply. Provides 4.7K-ohm isolation resistor on output.
8	+3.2V	MRIR +3.20 (+0.22V, -0.10V) regulator secondary supply. Provides a 4.7K-ohm isolation resistor on output.
9	----	Spare
10	RB4	208-cps symmetrical square wave output. Amplitude is $+0.2 \pm 0.1$ volts for the 1 state and $+2.0 \pm 0.5$ volts for the 0 state. Output impedance is greater than 4.7K ohms.
11	RB5	Pulse output that occurs every 4.8 milliseconds. Pulse duration for 1 state ( $+0.2 \pm 0.1$ volts) is 100 microseconds. For the remainder of the time, the 0 state is $+2.0 \pm 0.5$ volts. Output impedance is greater than 4.7K ohms.

Output Connector J4 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
12	RB1	1.66-kc symmetrical square wave output. Amplitude for 1 state is $+0.2 \pm 0.1$ volt and $+2.0 \pm 0.5$ volts for the 0 state. Output impedance is greater than 4.7K ohms.
13	RN4 (ECD)	20-microsecond pulse output which repeats every 4.8 milliseconds. Output amplitude is $+0.2 \pm 0.1$ volts for the 1 state and $+2.0 \pm 0.5$ volts for the 0 state. Output impedance is greater than 4.7K ohms.
14	<u>RK4</u>	25-kc symmetrical square wave output with an amplitude of $+2.0 \pm 0.5$ volts for the high level and $+0.2 \pm 0.1$ volts for the low level. The output impedance is greater than 4.7K ohms.

Output Connector J4 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
15	RC6	Pulse output that repeats 33 times per second. pulse duration is 4.8 milliseconds. Voltage amplitude is $+2.0 \pm 0.5$ volts for the 0 level and $+0.2 \pm 0.1$ volts for the 1 level. The output impedance is greater than 4.7K ohms.
16	RC1	Pulse output which occurs 30 milliseconds after C6 occurs. The voltage amplitude and output impedance characteristics are the same as C6 on Pin 15.
17	CH5	Radiometer Analog Input No. 5. This pin is provided for a protective purpose. During shipping this point is shorted to signal ground.
18	GRD S	Signal ground

Output Connector J4 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
19	GRD P	Power ground connected to the positive terminal of the satellite primary regulated supply.
20	-12 TMP	-12 volt telemetry point output. Nominal voltage output is -6 volts $\pm 4$ percent. The output impedance is 2.8K ohm $\pm 2$ percent.
21	CH4	Radiometer Analog Input No. 5. Same description as Pin 17 on this connector.
22	$\overline{\text{RD1}}$	LSB from the A/D data register. Voltage amplitude is $+2.0 \pm 0.5$ volts for the 0 state and $+0.2 \pm 0.1$ volts for the 1 state. Output impedance is greater than 4.7K ohms. Digital value is $2^0$ .
23	$\overline{\text{RD2}}$	$2^1$ Digital bit from the A/D data register. Voltage and impedance characteristics are the same as $\overline{\text{D1}}$ on Pin 22.



Output Connector J4 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
24	$\overline{RD3}$	$2^2$ Digital bit from the A/D data register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
25	$\overline{RD4}$	$2^3$ Digital bit from the A/D data register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
26	$\overline{RD5}$	$2^4$ Digital bit from the A/D data register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
27	$\overline{RD6}$	$2^5$ Digital bit from the A/D data register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
28	$\overline{RD7}$	$2^6$ Digital bit from the A/D data register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.

Output Connector J4 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
29	RD8	$2^7$ Digital bit from the A/D data register. Voltage and impedance characteristics are the same as $\overline{D1}$ on Pin 22.
30	CH3	Radiometer Analog Input No. 3. Same description as Pin 17 on this connector.
31	COMP OT	Comparator output voltage. Voltage output swings from +3.0 volts for $V_{\text{ladder}} < V_{\text{input}}$ to -6.0 volts for $V_{\text{ladder}} > V_{\text{input}}$ . Output impedance is greater than 4.7K ohms.
32	V PREC	Precision voltage output -10.0 $\pm$ 0.3 volts. Output impedance is greater than 4.7K ohms.
33	Spare	
34	CH2	Radiometer Analog Input No. 2. Same description as Pin 17 on this connector.

Output Connector J4 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
35	CH1	Radiometer Analog Input No. 1. Same description as Pin 17 on this connector.
36	GRD T	Telemetry ground
37	GRD C	Chassis ground

Input Connector J5

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
1	10 KC CLK	10-kc symmetrical square wave input nominal voltage swing is 0 volts to -6 volts. Input impedance is 3.3K $\pm$ 2 percent.
2	----	Spare
3	200 KC CLK	200-kc symmetrical square wave input. Nominal voltage swing is 0 volts to -6 volts. Input impedance is 24.7 ohms $\pm$ 10 percent.
4	GRD 200 KC	Provided as 200-kc input reference ground.
5	GRD P	Power ground connected to the positive terminal of the satellite primary regulated supply.
6	100 $\emptyset$ A	Input Phase A, 100 cps, square wave to be used by the radiometer subsystem. Nominal voltage swing is same as J3, Pin 9.

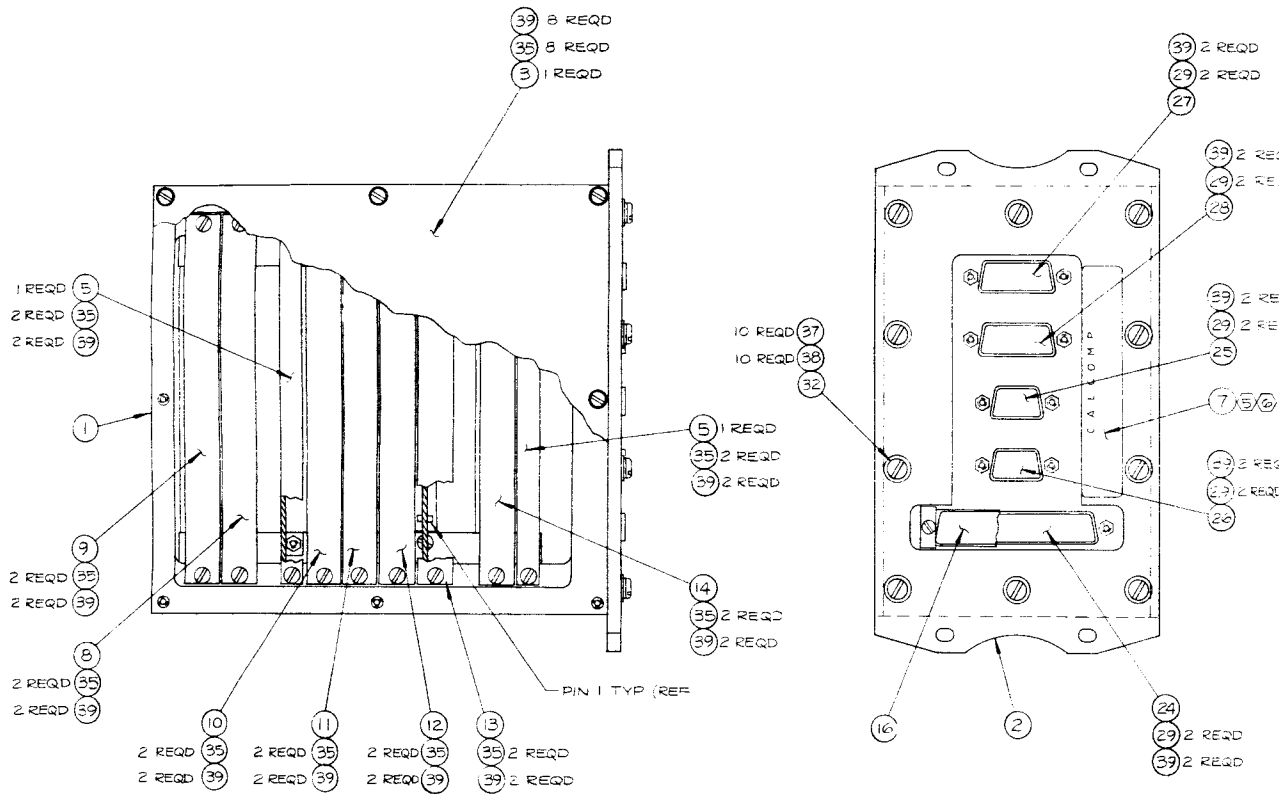
Input Connector J5 (continued)

<u>Pin</u>	<u>Term</u>	<u>Characteristics</u>
7	100 ØB	Input Phase B, 100 cps, square wave to be used by the Radiometer subsystem. Nominal voltage swing is same as J3, Pin 10. Phase B leads Phase A by 90 <sup>0</sup> .
8	----	Spare pin
9	GRD S	Signal ground

D0301-014

APPENDIX C

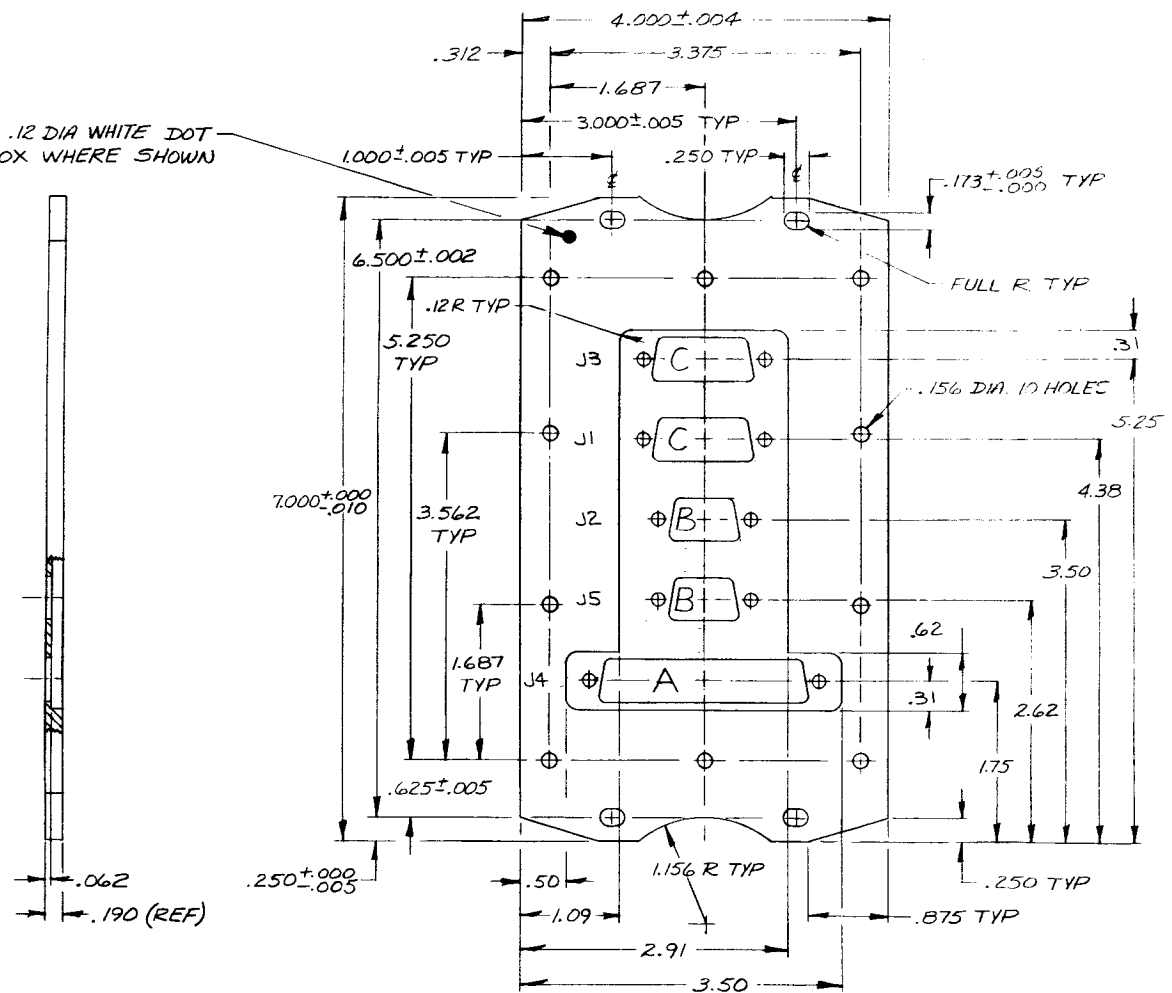
MRIR TELEMETRY UNIT  
MECHANICAL DRAWINGS



CALIFORNIA COMPUTER PRODUCTS INC.			
305 MULLER, ANAHEIM, CALIFORNIA			
MRIR-PCM			
DIGITAL SUB-SYSTEM			
SCALE: 1/1	SIZE F	10015-102	
DO NOT SCALE	WEIGHT	SHEET	OF 1

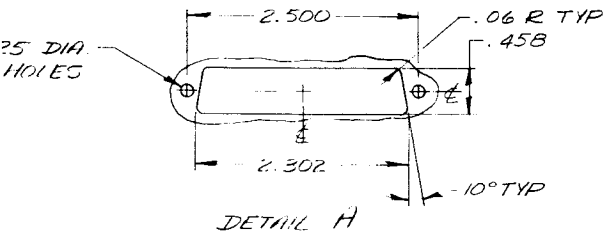
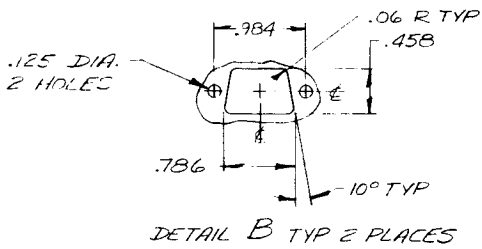
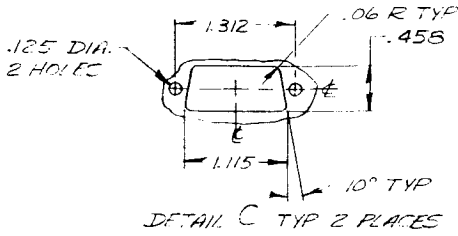


APPLY .12 DIA WHITE DOT  
APPROX WHERE SHOWN



5. TAG WITH PART NO. 63
  4. ALL MACHINED SURFACES
  - ① 3. DIM. #1 PER MIL. M.
  2. RUBBER STAMP DEC.
  1. MACHINE PER CCP SPEC.
- NOTE: UNLESS OTHERWISE SPECIFIED

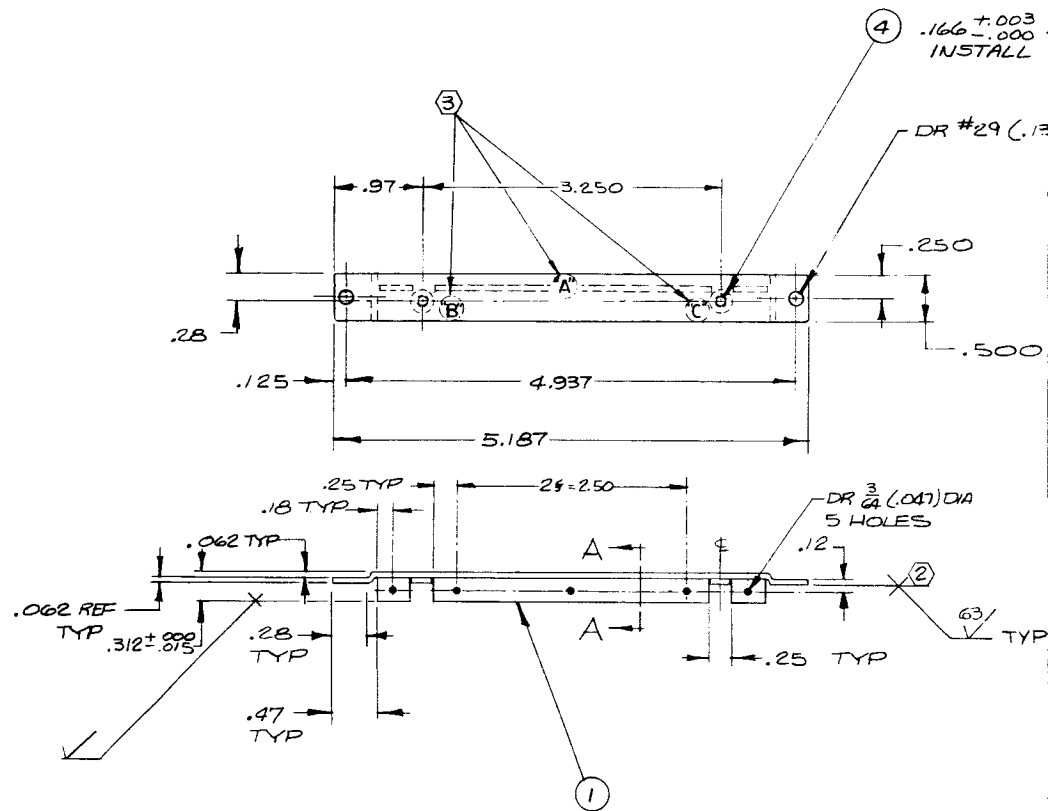
REVISIONS				DATE & APPROVAL	
SYM	ZONE	DESCRIPTION		DATE	APPROVAL
1		MAY BE REWORKED		2	CANNOT BE REWORKED
2		NONE			



1	11411-203	CONN. PLATE	.190 x 4.06 x 7.06	HP31E-HP6 MHS. (1)	2.5 M-44
REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION		ZONE
LIST OF MATERIAL OR PARTS LIST					
UNLESS OTHERWISE SPECIFIED		DRAWN	D. MILLER 2-28-65		
DIMENSIONS ARE IN INCHES		CHECK	E. HENNINGSEN 1-21-66		
TOLERANCES ON		APPD	2-11-66		
DECIMALS		APPD	2-11-66		
XX ± .03		FINISH			
XXX ± .010		HEAT TREAT			
DRILLED HOLES		SURFACE ROUGHNESS PER MIL-STD-10			
.040 TO .1285: +.002, -.001		✓			
.136 TO .228: +.003, -.001		SCALE: FULL			
.234 TO .500: +.004, -.001		SIZE D			
.515 TO .750: +.005, -.001		WEIGHT			
.765 TO 1.000: +.007, -.001		SHEET 1 OF 1			
1.015 TO 2.000: +.010, -.001		DRAWING NO. 11411-203			

2

DASH NO	"A" (3)	"B" (3)	"C" (3)
-11	ANALOG INPUTS & 25KC	ASSY NO 10351-502	SERIAL NO (4)
-21	ENCODE-TIMING	ASSY NO 10353-502	SERIAL NO (4)
-31	FRAME SYNC OUTPUT	ASSY NO 10355-502	SERIAL NO (4)
-41	A/D DATA CONTROL	ASSY NO 10365-502	SERIAL NO (4)
-51	A/D CONVERTER	ASSY NO 10367-502	SERIAL NO (4)
-61	DC/DC CONVERTER #1	ASSY NO 10370-502	SERIAL NO (4)
-71	DC/DC CONVERTER #2	ASSY NO 10371-502	SERIAL NO (4)



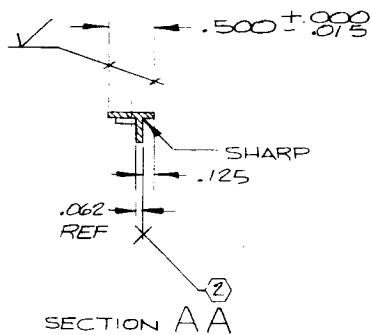
- ⑥ 10. PENN ENG'G & MFG CO.
  - ⑤ 9. MAKE FROM PA 6530 PIONEER ALLIM, LOS AN
  - ④ 8.
  - ③ 7. TO BE ASSIGNED
  - ② 6. ELECTRO-ETCH DESIGN WHERE SHOWN USING .125
  - ① 5. ALL MACHINE SURFACES
  - ② 4. NORMAL WITHIN .005 IN
  - ③ 3. BREAK SHARP EDGES .01
  - ① 2. CAUSTIC DIP AFTER
  1. MACHINE PER CCP SPEC
- NOTE: UNLESS OTHERWISE

SYM		ZONE		REVISIONS		DATE & APPROVAL	
				DESCRIPTION			
				1 MAY BE REWORKED 2 CANNOT BE REWORKED			
				3 NONE			
4		A		1. IN TAB BLOCK; -G1 DC/DC CONV. #1 WAS POWER SUPPLY #1, -71 DC/DC CONV. #2 WAS POWER SUPPLY #2 -G1 DC/DC CONV. #1, ASSY NO 10370-502 WAS 10369-502 (EO 1341) EFFECT ON: UNIT #2 & SUBS		ARC 4-21-66	
						COM	

DIA 2 HOLES  
FARSIDE

G) 2 HOLES

REF



6	4	2	2	2	2	2	2	2	CLS-440-2	NUT, CLINCH				COM'L	
5	1	1	1	1	1	1	1	1	11412-203-1	TEE		(5)	(5)	COM'L	
ITEM	-71	-61	-51	-41	-31	-21	-11		11412-203	TEE, P.C.B.					
NO	REQD	REQD	REQD	REQD	REQD	REQD	REQD		PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION			ZONE	

DOYLESTOWN, PA.  
X 5.25, G682-T5 AL ALY EXT.  
SELES, CALIFORNIA.

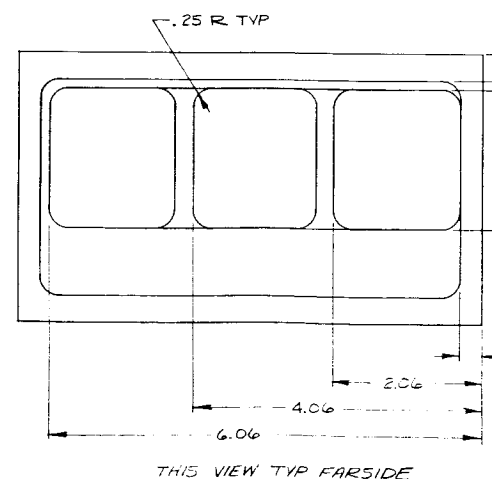
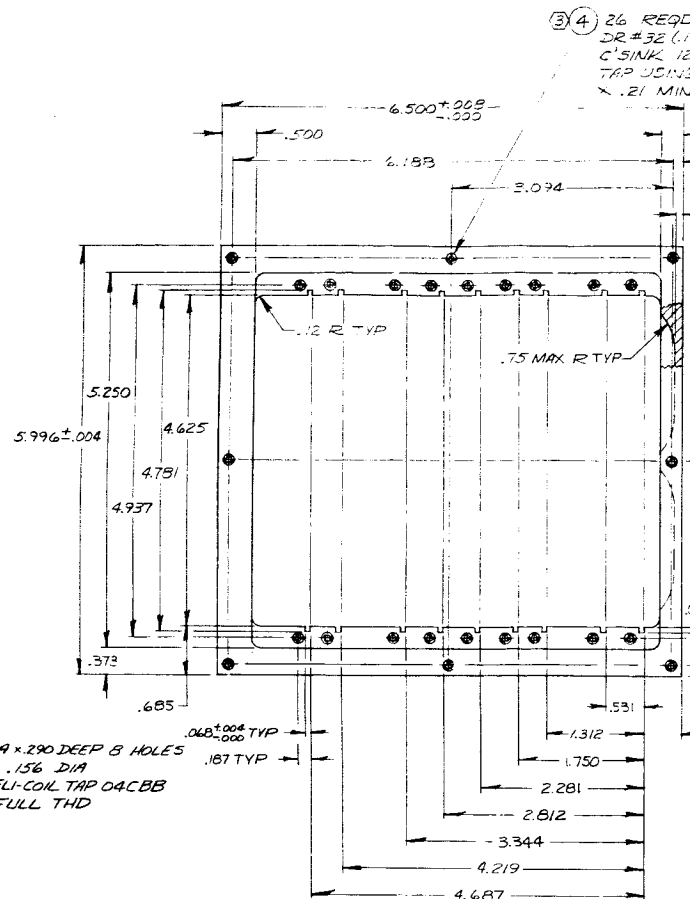
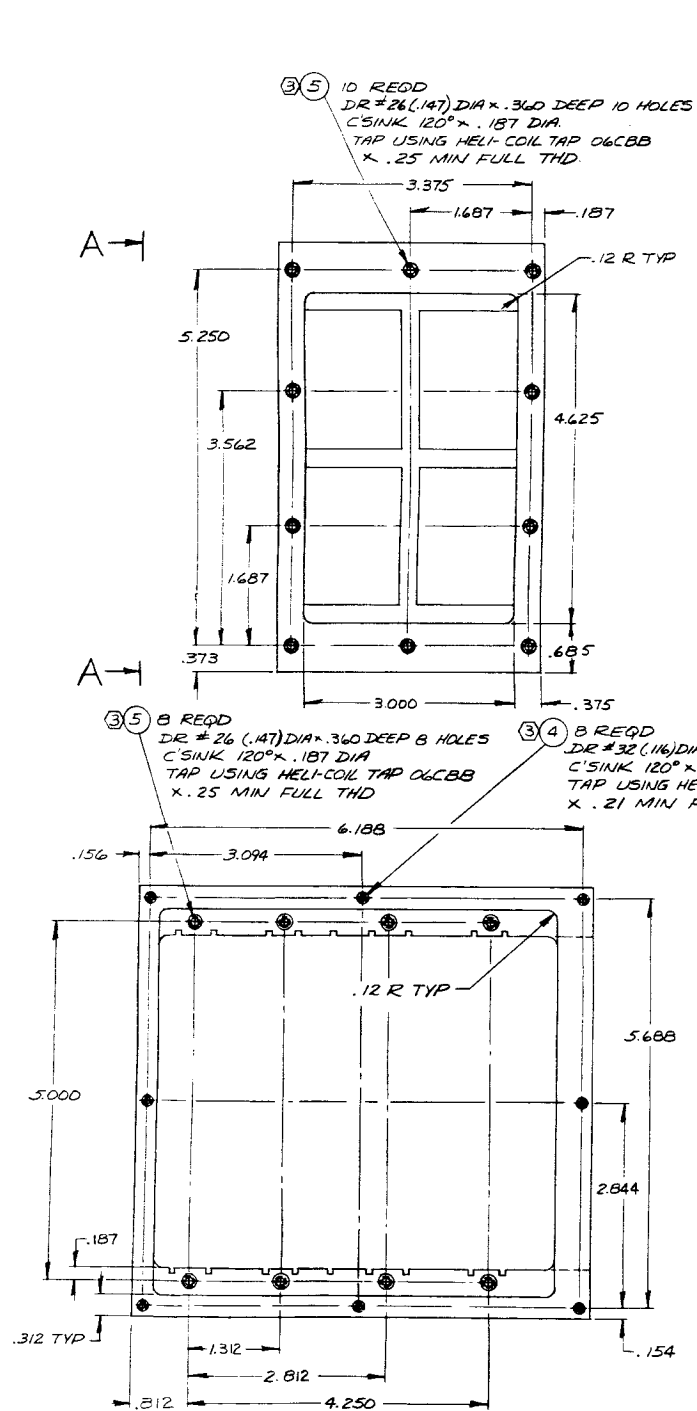
TURNS APPROX  
HIGH CHARACTERS.  
1. TYP BOTH ENDS.  
3-015.  
ELECTRO-ETCHING.  
40102-001.  
SPECIFIED

UNLESS OTHERWISE SPECIFIED		LIST OF MATERIAL OR PARTS LIST	
DIMENSIONS ARE IN INCHES		DRAWN	12-29-65
TOLERANCES ON		CHECK	1-21-66
DECIMALS	ANGLES	APPD	2-1-66
.XX ± .03	± 0° 30'	APPD	2-1-66
.XXX ± .010		FINISH	①
DRILLED HOLES		HEAT TREAT	
.040 TO .1285: +.002, -.001		SURFACE ROUGHNESS PER MIL-STD-10	✓
.136 TO .228: +.003, -.001			
.234 TO .500: +.004, -.001		SCALE:	1
.515 TO .750: +.005, -.001		SIZE	D
.765 TO 1.000: +.007, -.001		DO NOT SCALE THIS DRAWING	11412-203
1.015 TO 2.000: +.010, -.001		WEIGHT	
		SHEET	

CALIFORNIA COMPUTER PRODUCTS INC.  
305 MULLER, ANAHEIM, CALIFORNIA

TEE-PC.B ASSY

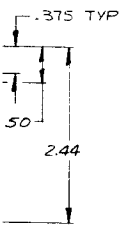
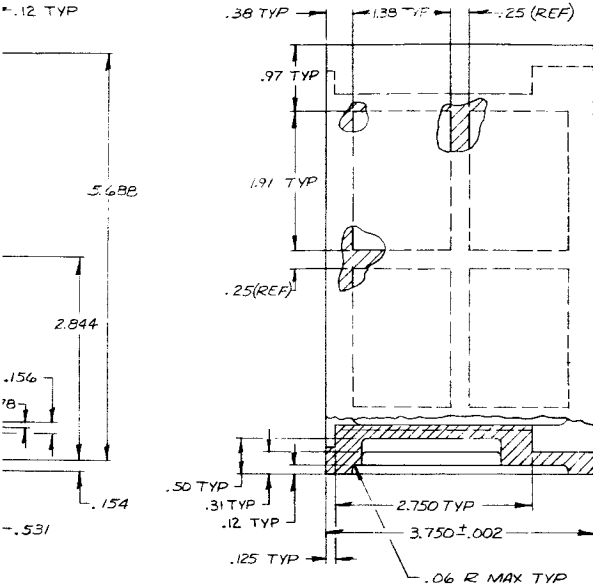
2



SYN		ZONE		REVISIONS		DATE & APPROVAL	
				DESCRIPTION			
				1 MAY BE REWORKED		2 CANNOT BE REWORKED	
				3 NONE			

6) DIA. X .030 DEEP 24 HOLES  
 0° X .156 DIA  
 HELI-COIL TAP 04CBB  
 FULL THD.

-.312  
 -.156



-.31 TYP

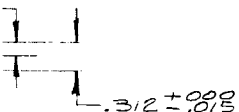
ITEM	1	11413-203	HOUSING, PCB	900 DIA. X 3.81	ZK60A-T5 MAG ALY	QQ-M-31	ZONE														
NO	REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION			ZONE														
LIST OF MATERIAL OR PARTS LIST																					
UNLESS OTHERWISE SPECIFIED		DRAWN	D. MILLER 12-29-65																		
DIMENSIONS ARE IN INCHES		CHECK	B. MILLER 2-1-66																		
TOLERANCES ON		APPD	B. MILLER 2-1-66																		
DECIMALS		APPD	B. MILLER 2-1-66																		
ANGLES		FINISH	②																		
XX ± .03		HEAT TREAT																			
XXX ± .010																					
DRILLED HOLES																					
.040 TO .125: +.002, -.001																					
.136 TO .228: +.003, -.001																					
.234 TO .500: +.004, -.001																					
.515 TO .750: +.005, -.001																					
.765 TO 1.000: +.007, -.001																					
1.015 TO 2.000: +.010, -.001																					
SURFACE ROUGHNESS PER MIL-STD-10		✓		DO NOT SCALE THIS DRAWING																	
CALIFORNIA COMPUTER PRODUCTS INC. 305 MULLER, ANAHEIM, CALIFORNIA				HOUSING P.C.B. MRIR-PCM																	
SCALE: FULL				SIZE F		11413-203															
WEIGHT				SHEET 1 OF 1																	

6) DIA. X .030 DEEP 24 HOLES  
 0° X .156 DIA  
 HELI-COIL TAP 04CBB  
 FULL THD.  
 NOTE: UNLESS OTHERWISE SPECIFIED

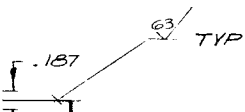
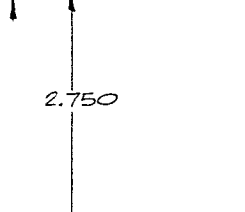



7. IDENTIFY  
(2) 6. MAKE FROM  
GOG3-T5  
PIONEER AD  
125  
5. ✓ ALL MA  
4. FABRICATE  
3. BREAK SHA  
(1) 2. CAUSTIC  
1. MACHINE PER  
NOTE: UNLESS


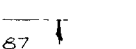
REVISIONS				DATE & APPROVAL	
SYM	ZONE	DESCRIPTION		DATE	APPROVAL
		1	MAY BE REWORKED	2	CANNOT BE REWORKED
		3	NONE		


  
 $.312 \pm .003$ 
  
 #29 (.136) 2 HOLES

3


  
 $.187$ 
  
 $\phi .312$  TYP
   

  
 2.750
   

  
 $.187$  TYP
   
 R TYP

9
   
 7 REF


  
 $.312$ 
  

  
 $.187$

$\frac{1}{8}$  (.125) DIA
   
 HOLES

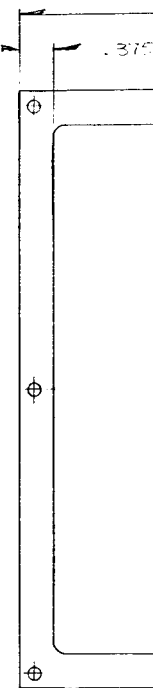
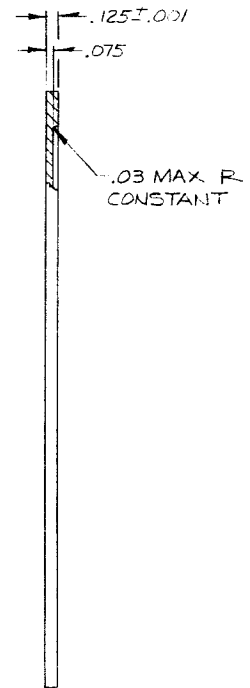
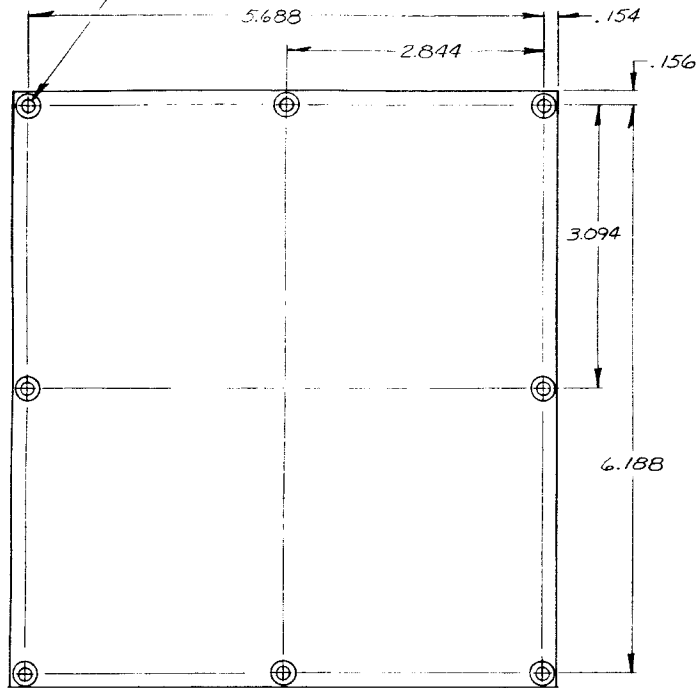
PER CCP SPEC AO104-CCI.
   
 M PA 6530 X 5.25
   
 AL ALY EXT.
   
 IM, LOS ANGELES, CALIFORNIA.
   
 MACHINE SURFACES.
   
 PER CCP SPEC AO103-CCI
   
 P EDGES .010-.015.
   
 DIP.
   
 CCP SPEC AO102-CCI.
   
 OTHERWISE SPECIFIED

5	4	M520426A02-4	RIVET				
3	1	11414-203-5	TEE	(2)	(2)		
1	1	11414-203-3	SHIELD	06 X 3.18 X 4.81	5052 H32 ALALY SHI	QQ-A-318c	
ITEM	1	11414-203	SHIELD - PCB				
NO.	REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION			ZONE
LIST OF MATERIAL OR PARTS LIST							
UNLESS OTHERWISE SPECIFIED			DRAWN	CALIFORNIA COMPUTER PRODUCTS INC.			
DIMENSIONS ARE IN INCHES			CHECK	305 MULLER, ANAHEIM, CALIFORNIA			
TOLERANCES ON			APPD	SHIELD - P.C.B. MRIR P.C.M.			
DECIMALS			APPD				
ANGLES			FINISH				
.XX ± .03			HEAT TREAT				
XXX ± .010			SURFACE ROUGHNESS PER MIL-STD-10				
DRILLED HOLES			SCALE: $\frac{1}{1}$				
.040 TO .1285: +.002, -.001			SIZE D				
.136 TO .228: +.003, -.001			11414-203				
.234 TO .500: +.004, -.001			DO NOT SCALE THIS DRAWING				
.515 TO .750: +.005, -.001			WEIGHT				
.765 TO 1.000: +.007, -.001			SHEET				
1.015 TO 2.000: +.010, -.001							

2

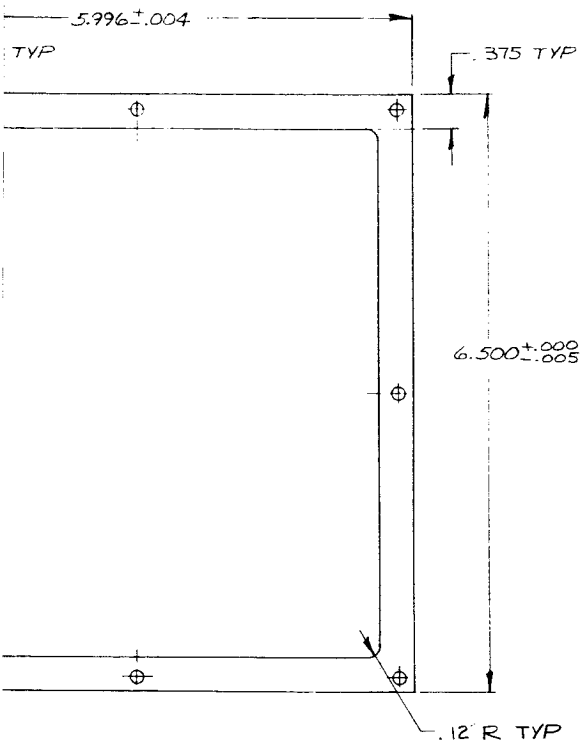


DR  $\frac{1}{8}$  (.125) DIA B HOLES  
 C-BORE .250 DIA X .078 $\pm$ .005 DEEP  
 .010 MAX FILLET RADII



3. TAGS WITH PART  
 ① 2. DOW #17 PER  
 1. MACHINE PER  
 NOTE: UNLESS OTHERWISE SPECIFIED

REVISIONS				DATE & APPROVAL	
SYM	ZONE	DESCRIPTION		DATE	APPROVAL
		1	MAY BE REWORKED	2	CANNOT BE REWORKED
		3	NONE		



1	11415-203	COVER	.160 x 6.06 x 6.56	A231B-H24 MAS. ALY	QQ-M-44	
REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION		ZONE	
LIST OF MATERIAL OR PARTS LIST						
UNLESS OTHERWISE SPECIFIED		DRAWN	D. MILLER	12-29-65	CALIFORNIA COMPUTER PRODUCTS INC.	
DIMENSIONS ARE IN INCHES		CHECK	E. HENNINGSON	1-21-66	305 MULLER, ANAHEIM, CALIFORNIA	
TOLERANCES ON		APPD	E. HENNINGSON	2-1-66	COVER, HOUSING MRIR-PCM	
DECIMALS		APPD	E. HENNINGSON	2-1-66		
ANGLES		FINISH	①			
XX ± .03		HEAT TREAT		SCALE:	SIZE	11415-203
XXX ± .010		SURFACE ROUGHNESS PER MIL-STD-10		FULL	D	
DRILLED HOLES		DO NOT SCALE THIS DRAWING		WEIGHT	SHEET 1 OF 1	
.040 TO .1285: +.002, -.001						
.136 TO .228: +.003, -.001						
.234 TO .500: +.004, -.001						
.515 TO .750: +.005, -.001						
.765 TO 1.000: +.007, -.001						
1.015 TO 2.000: +.010, -.001						

ND. PER CCP SPEC A0104-001  
2 MIL-M-45202 TYPE I, CLASS C  
2 CCP SPEC A0102-001  
HERWISE SPECIFIED

2



1492		REVISIONS			
SYM	ZONE	DESCRIPTION		DATE & APPROVAL	
		1	MAY BE REWORKED	2	CANNOT BE REWORKED
		3	NONE		

1  
3 (.125) DIA  
HOLES

-.125 THICK

45° X .09 TYP  
2 PLACES

5  
32 (.156) DIA  
HOLES

1		11416-203	PLATE-MTG	.125 X .875 X 3.250	431B-H24 MAG. ALY	QQ-M-44	
REQD	PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION	MATERIAL SIZE, DESCRIPTION & SPECIFICATION			ZONE
LIST OF MATERIAL OR PARTS LIST							
UNLESS OTHERWISE SPECIFIED		DRAWN	A.R. COLL	12-30-65	CALIFORNIA COMPUTER PRODUCTS INC. 305 MULLER, ANAHEIM, CALIFORNIA  PLATE-MTG. CONN. MRIR-PCM		
DIMENSIONS ARE IN INCHES		CHECK	B. Heney	1-21-66			
TOLERANCES ON		APPD	D. Miller	2-1-66			
DECIMALS		APPD	D. Plush	2-1-66			
ANGLES		FINISH					
XX ± .03		HEAT TREAT			SCALE:		
XXX ± .010		SURFACE ROUGHNESS PER MIL-STD-10			SIZE		
DRILLED HOLES					C		
.040 TO .1285: +.002, -.001					11416-203		
.136 TO .228: +.003, -.001					WEIGHT		
.234 TO .500: +.004, -.001					SHEET		
.515 TO .750: +.005, -.001							
.765 TO 1.000: +.007, -.001							
1.015 TO 2.000: +.010, -.001							

2

D0301-014

APPENDIX D

MRIR TELEMETRY UNIT

PIN CHART

J004		
J107-Y	RELAY TP	1
J107-L	TEMP TMP	2
		3
J107-07	-18.0V TP	4
J107-01	-12.0V TP	5
J107-09	-6.0V TP	6
J107-08	6.0V TP	7
J107-10	3.2V TP	8
		9
J104-16	RB4	10
J104-13	RB5	11
J104-15	RB1	12
J104-04	RK4	13
J101-E	RK4	14
J101-D	RC6	15
J101-20	RC1	16
J101-13	CH5	17
J106-V	GRD S	18
J102-05	GRD P	19
J107-02	-12.0V TMP	20
J101-12	CH4	21
J103-14	RD1	22
J103-15	RD2	23
J103-20	RD3	24
J103-18	RD4	25
J103-17	RD5	26
J103-06	RD6	27
J103-03	RD7	28
J103-E	RD8	29
J101-S	CH3	30
J102-12	COMP OT	31
J102-22	V.PREC	32
		33
J101-14	CH2	34
J101-U	CH1	35
J102-09	GRD T	36
CHB	GRD C	37

J001		
J003-2	24.5 RDA	2
		3
J106-20	OFF CMD	4
J106-22	OFF CMDR	5
		6
J106-Y	GRD S	7
J102-06	GRD P	8
J106-17	24.5V M	9
J107-R	24.5V TM	10
J106-21	ONCMD	11
J106-19	ONCMDR	12
		13
J102-10	GRD T	14
CHA	GRD C	15

J005		
J104-X	10 KC	1
		2
J101-C	200 KC	3
J101-B	200 KC GRD	4
J102-05	GRD P	5
J003-09	100 $\phi$ A	6
J003-10	100 $\phi$ B	7
		8
J106-V	GRD S	9

J002		
J105-11	TRO1	1
		2
J105-13	GRD TRO1	3
J105-9	GRD TRO2	4
J102-06	GRD P	5
J105-06	TRO2	6
J106-W	GRD S	7
J102-09	GRD T	8
CHB	GRD C	9

J003		
J106-18	24.5V MR	1
J001-02	24.5V RDA	2
		3
J101-U	CH1	4
J004-34	CH2	5
J101-14	CH3	6
J106-Y	GRD S	7
J102-07	GRD P	8
J005-06	100 $\phi$ A	9
J005-07	100 $\phi$ B	10
		11
J004-21	CH4	12
J101-12	CH5	13
J102-10	GRD T	14
CHA	GRD C	15

# ANALOG INPUTS # 25 KC GEN J101

	1	A	GRD S	J101-06
	2	B	200 KC GRD	J101-F
	3	C	200 KC	J005-04
	4	D	RC6	J005-03
	5	E	RK4	J004-15
	6	F	GRD S	J004-14
J101-A	GRD S	7	H	R4
	8	J		J101-Z
	9	K	C6	J104-02
J103-V	K4C	10	L	
	C5	11	M	K4
J003-12	CH4	12	N	3.2V
J004-21	CH5	13	P	VCHO
J003-13	CH2	14	R	
J004-34	VCHO	15	S	CH3
J003-05		16	T	-18V
J101-P		17	U	CH1
J104-18	B4C	18	V	VCHO
J105-H	C1	19	W	
		20	X	C6
J004-16	RC1	21	Y	
J105-04	C1	22	Z	GRD S
J101-K	C6			J101-K
				J104-10
				J101-F

# A/D CONVERTER J102

J102-01	D7	1	A	GRD S	J102-14
J103-02	DB	2	B		J104-02
INTERNAL TEST POINT	V COMP	3	C		
		4	D		
J004-19	GRD P	5	E		
J005-05	GRD P	6	F	-12V	J107-B
J002-05	GRD P	7	H		
J003-08	GRD P	8	J		
J106-Z		9	K		
J002-08	GRD T	10	L	D5	J103-19
J001-14		11	M	-6V	J103-L
J003-14	COMP OT	12	N	D6	J103-D
J004-31	VCHO	13	P	3.2V	J101-N
J103-H	GRD S	14	R	6.0V	J103-05
J101-V	VREF	15	S		J104-R
J102-A		16	T		
J102-Z		17	U	-18V	J101-T
INTERNAL TEST POINT		18	V		J107-12
J103-21		19	W		
J103-22		20	X		
J103-K		21	Y		
		22	Z	GRD S	J102-14
J103-11					
J004-32	V.PREC				

# FRAME SYNC # DATA OUTPUT J105

J104-M	B1C	1	A	GRD S	J104-07
J104-N	3.2V	2	B	EB	J105-Z
J105-N	EB	3	C		
	C1	4	D		
J101-21	D7	5	E		
J103-01	TRO2	6	F		
J002-06	DB	7	H	C1	J101-18
J103-02	D6	8	J		
J103-D	GRD TRO2	9	K		
J002-04	D5	10	L	-6V	J104-L
J103-19	TRO1	11	M		J107-11
J002-01		12	N	3.2V	J105-02
		13	P		J107-M
J002-3	GRD TRO1	14	R	6V	J104-R
		15	S		J107-13
J103-22	D4	16	T		
J103-21	D3	17	U		
J103-11	D2	18	V		
J103-13	D1	19	W	A1	J104-P
	F	20	X	H	
J104-14	B1	21	Y	B5	J104-17
	F	22	Z	GRD S	J105-A

# DC/DC CONVERTER J106

	1	A		
	2	B		
	3	C		
	4	D		
J107-05	32V UNREG	5	E	
		6	F	
		7	H	
		8	J	
		9	K	
		10	L	
		11	M	
		12	N	
		13	P	
		14	R	
J107-15	6V UNREG	15	S	
		16	T	
J001-09	24.5V M	17	U	
J003-01	24.5V MR	18	V	
J107-18	ONCMDR	19	W	
J001-12	OFF CMD	20	X	
J001-04	ON CMD	21	Y	
J101-11	OFF CMDR	22	Z	

A/D DATA CONTROL J103					ENCODE-TIMING GEN J104							
22-01	D7	1	A	GRD S	J103-Z	J104-08	J101M	K4	1	A	GRD S	J104-06
25-05							J101H	K4	2	B	N4	J103-U
22-02	D8	2	B	S8	J103-04				3	C		
5-07	RD7	3	C	3.2V	J103-05	J103-N	J004-13	RN4	4	D		
4-23	S8	4	D	D6	J102-N	J105-08			5	E		
25-B	3.2V	5	E	RD8	J004-29		J104-A	GRD S	6	F		
22-P		6	F	1DB	J103-J		J104-Y	GRD S	7	H	B1	J105-20
23-C	RD6	7	H	COMP OT	J102-12		J105-A	GRD S	8	J		
	S8	8	J	1DB	J103-F		J103-A	GRD S	9	K		
		9	K	D1A	J102-18		J102-A	GRD S	10	L	-6V	J103-L
		10	L	-6V	J102-L		J101-Z	GRD S	11	M	B1C	J105-L
2-21	D2	11	M		J104-L		J106-V	GRD S	12	N	3.2V	J105-O1
5-17		12	N	3.2V	J103-C				13	P	A1	J103-N
		13	P		J104-N		J004-11	RB5	14	R	6V	J105-O2
5-18	D1	14	R				J105-21	B1	15	S		J105-W
4-22	RD1	15	S				J004-12	RB1	16	T		J102-R
4-23	RD2	16	T				J004-10	RB4	17	U		J105-R
		17	U	N4	J104-B		J105-Y	B5	18	V		
24-26	RD5	18	V	K4C	J101-10		J101-17	B4C	19	W		
24-25	RD4	19	W						20	X	10KC	J005-01
2-L	D5	20	X						21	Y	GRD S	J104-A
5-10	RD3	21	Y						22	Z	GRD S	
24-24	D3	22	Z	GRD S								
2-16	D4											
25-16												
2-17												
25-15												

1560		REVISIONS		DATE & APPROVAL	
SYM	ZONE	DESCRIPTION		DATE & APPROVAL	
		1	MAY BE REWORKED	2	CANNOT BE REWORKED
			3	NONE	

REVISIONS				DATE & APPROVAL	
REV	ZONE	DESCRIPTION			
1		MAY BE REWORKED	2	CANNOT BE REWORKED	
3		NONE			

NO. 1		DC/DC CONVERTER NO.2 J107						
RD P	J106-Z J107-A	J004-05	-12V TP	1	A	GRD P	J107-Z J106-A	
		J004-20	-12V TMP	2	B	-12V	J102-F	
				3	C			
				4	D			
		J106-05	3.2V UNREG	5	E			
				6	F	FLXO IN	J106-F	
O IN	J107-F	J004-04	-18V TP	7	H	-6V UNREG	J106-H	
UNREG	J107-H	J004-07	6V TP	8	J			
		J004-06	-6V TP	9	K	-12V UNREG	J106-K	
UNREG	J107-K	J004-08	3.2V TP	10	L	TEM TMP	J004-02	
		J105-L	-6V	11	M	3.2V	J105-N	
		J102-U	-18V	12	N			
		J105-R	6V	13	P			
				14	R	-24.5V TM	J001-10	
		J106-15	6V UNREG	15	S			
				16	T	-18V UNREG	J106-T	
				17	U			
		J106-18	-24.5V MR	18	V			
ID S	J004-18			19	W			
ID S	J005-09			20	X			
ID S	J002-07			21	Y	RLY TMP	J004-01	
ID S	J104-11			22	Z	GRD P		
ID S	J001-07							
ID P	J106-A J102-07							

1 10403-502		PIN CHART		MATERIAL		ZONE	
REDD		PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION		SIZE, DESCRIPTION & SPECIFICATION	
UNLESS OTHERWISE SPECIFIED				LIST OF MATERIAL OR PARTS LIST			
DIMENSIONS ARE IN INCHES				DRAWN 2/1/66 4-29-66			
TOLERANCES ON				CHECK 2/1/66 5-3-66			
DECIMALS				APPD 2/1/66 5-16-66			
ANGLES				FINISH			
XX ± .03				HEAT TREAT			
XXX ± .010				SURFACE ROUGHNESS PER MIL-STD-10			
DRILLED HOLES				SCALE: NONE			
.060 TO .125 ± .002, -.001				SIZE: F			
.125 TO .250 ± .002, -.001				WEIGHT			
.250 TO .375 ± .002, -.001				SHEET			
.375 TO .500 ± .002, -.001							
.500 TO .750 ± .002, -.001							
.750 TO 1.000 ± .002, -.001							
1.000 TO 2.000 ± .002, -.001							